Signaling Techniques for NoC

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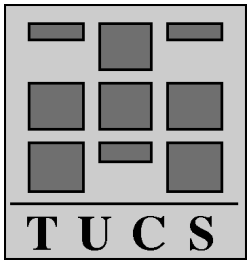

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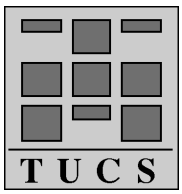

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Abstract

The gate length of a few tens of a nanometer for CMOS has become a distinct possibility due to technology scaling. Furthermore, the amount of transistors in a single die is increasing steadily over time towards gigascale integration (GSI) level. This development creates a noise and power dissipation problems into a system design. In addition to this, signaling over nanometer interconnects represents a major bottleneck in ULSI systems due to the dominant limitation of signal propagation delays. To a large extent, the on-chip signaling technique determines the reliability, speed, and power consumption of a network-on-chip (NoC). An efficient on-chip signaling scheme is the one that maximizes the data rate per pin, minimizes power dissipation, and provides good noise immunity. Such signaling convention can dramatically increase available data rate and hence system performance.

Three signaling techniques, namely voltage- and current-mode differential signaling and simultaneous current-mode bidirectional signaling, were selected from the on-chip signaling scheme, which has a promising feature for the future technology scaling impact as a case study. Interconnects were modeled using transmission line model from Spectre and lumped RC-model. For the latter, the length of the interconnect varied from 0.1 mm to 3 mm. Finally, a 32-bit bus was constructed by utilizing the above mention techniques. Simulation and performance analysis was carried out for 0.18 μm technology.

Keywords: signaling, interconnect, noise, power consumption

TUCS Laboratory
Communication Systems Laboratory

1 Introduction

By looking a few years ahead, a single-chip or single-package system in 2010 will be a fault-tolerant, on-chip distributed real-time system consisting of up to a hundred resources communicating over a sophisticated communication infrastructure. Typical individual resources will be processor cores, memories, configurable logic blocks, optimized digital single-function blocks, and mixed-signal interface blocks. In modern network-on-chip (NoC) design, a significant effort has to be invested to optimization of on-chip communication links between system modules and to verification of overall functionality and timing. This is because performance, reliability, and also power consumption of the system strongly depend on the implementation of module interconnects [8].

A signaling technique involves in encoding information into current or voltage, generating a reference against which this quantity is measured, providing terminations to couple signal energy into the transmission medium and absorb energy to prevent unwanted reflections, and controlling signal transitions to limit the spectrum of transmitted energy [1]. An efficient signaling scheme is the one that maximizes the data rate per pin, minimizes power dissipation, and provides good noise immunity [5]. Such signaling convention can dramatically increase available data rate and hence system performance.

This report will focus on implementing three signaling conventions for NoC-interconnects, namely differential current- and voltage-mode signaling and current-mode bidirectional signaling. These techniques were selected among the existing signaling scheme, of which has a promising feature for the future technology scaling impact. Performance analysis was carried out for power consumption, speed and reliability. Three types of simulation was performed, firstly, a transmission line model from Spectre AnalogLib is used to model the interconnect between the transmitter/receiver pairs. Secondly, a lumped RC-model is utilized as an interconnect model, with variable lengths. Finally, a 32-bit bus is constructed, by applying the signaling techniques presented above.

The noise sources in signaling are presented in Section 2, emphasizing power supply noise and crosstalk. The basics of the voltage- and the current-mode signaling are described in Section 3. Section 4 and Section 5 concentrates on differential and simultaneous bidirectional signaling, respectively. Analysis of these signaling conventions is found in Section 6. Conclusion of the work is presented in Section 7.

2 Noise in Signaling

Noise in digital systems is mainly due to internal sources such as current flowing through parasitic components, in the power supply network, parasitic coupling between signal lines, signal line ringing, shared signal returns, and device parameter variations [6]. The intended signal, V_S, might be corrupted with a number of noise sources, which results the received signal $V_R = V_S + V_N$ where V_N present the noise [1, 6]. Large amount of system created noise is induced by transmission of the signals and scales with the signal magnitude. Noise can be divided into two components, as shown in equation 1.

$$V_N = K_N V_S + V_{NI} \tag{1}$$

The first component present those noise sources that are proportional to signal magnitude, such as crosstalk and signal induced power supply noise. While the latter component present sources that are independent to signal magnitude, for instance transmitter- and receiver offsets.

2.1 Power Supply Noise

Power supply noise or unwanted fluctuation of the supply voltage within a digital ULSI chip mainly originates from simultaneous switching of CMOS circuits which causes high peak current draws from the power source. The total power supply noise is the sum of two major components: the resistive voltage drop IZ and the inductive switching noise $L\Delta I/\Delta t$ [4]. Here R and L are the effective supply wire resistance and inductance, respectively, and ΔI is the total current change during the rise or fall time Δt of the concurrently transitioning signals.

Large common-mode voltage fluctuations between power supplies in different parts of the network can cause signal undershoots at the receiver [6]. Voltage shifts, as well as IZ drops and signal ringing, corrupt signals that use a power supply as either transmit or receive voltage reference, or both. In a well designed digital system, power supply noise is managed through a combination of reduction and isolation. The noise is minimized by careful design of the distribution network and the use of bypass capacitors. The effect of supply noise is minimized by choosing a signaling convention that is less insensitive [7] to power supply noise, e.g. current-mode signaling.

To determine the required signal swing or analyze the noise immunity of a signaling system, the power supply noise which is generated by the signaling system should be separated from that generated by other sources. A well designed signaling system contributes very little to the supply noise by using

small swings and either drawing a constant DC current from the supply or controlling rise times to minimize interaction with the supply inductance. A poorly designed, brute-force signaling system, however, can generate significant amounts of supply noise by driving large voltage swings into large capacitive loads with short rise times in an unbalanced manner.

2.1.1 Single Supply Noise

Spatial variation in a single supply (GND or Vdd) between two point is called single supply noise [6]. The single supply noise between two points in a supply network is generally an increasing function of the distance between the two points, because the supply impedance between these points increases with distance. When employing voltage mode signaling by using a supply as a reference, this noise is directly added to the signal. By adopting differential signaling or introducing an explicit reference, the single supply noise is made common-mode and is mostly rejected [3]. One approach to deal with it is to operate with current mode signaling conventions.

2.1.2 Differential Supply Noise

A variation between two supplies (Vdd and GND) is denoted as a differential supply noise. It is caused by IZ drops in both supply networks back to a reference point [1]. It can be controlled through a combination of reduced supply impedance, bypass capacitors, supply isolation, and local regulation. Because most signals are referenced to a single supply, they are less sensitive to differential supply noise than they are to single supply noise. However, when signals referenced to one supply are capacitively coupled to the other supply, differential supply noise is coupled into the signal. Delay is a major concern with differential supply noise.

2.2 Crosstalk

Crosstalk has become a major source of noise in high-speed integrated circuits because of the non-proportional scaling of vertical and horizontal dimensions of interconnects and decreasing wire pitch. Crosstalk has two major detrimental effects [6]. First, if the magnitude and duration of the coupled noise is sufficient, a signal may temporarily assume an erroneous logic value which in turn may lead to a logical failure. Secondly, crosstalk also affects timing. The delay of a wire not only depends on the properties of the wire itself but also on how the wires that are capacitively or inductively coupled to it are switching. If a wire and another wire coupled to it switch simultaneously in

opposite directions, crosstalk increases the delay of the wires because twice as much charge must be transferred across the coupling capacitance. On the other hand, if the coupled wires switch in the same direction, the delay is reduced. On-chip crosstalk is primarily caused by capacitive coupling of nearby signals. A transition on a signal injects charge into adjacent signals, disturbing their voltage. Off-chip transmission lines are coupled by mutual inductance as well as capacitance.

Crosstalk between transmission lines may induce traveling waves to nearby transmission lines owing to parasitic capacitance and mutual inductance between the lines [8]. Whenever a pair of signals, A and B, share a return path that has finite impedance, a transition on signal A induces a voltage across the shared return impedance that appears as noise on signal B. In a typical system, shared wire bonds, package pins, board planes and traces, connector pins, and cables all contribute to the impedance, largely to inductance of the signal return. Unless differential signaling is used, or each signal is supplied with its own return, signals share returns, and crosstalk over these returns is a major source of noise. Sending balanced currents, as with differential signaling, completely eliminates signal return crosstalk. In cases where the supply and ground are used as signal returns, the increase in local ground voltage due to signal-return crosstalk across lead inductance is sometimes referred to as "ground bounce".

If the characteristics of the transmission lines and the shared return impedance are known, signal return crosstalk can in principle be predicted and canceled at the sending end. Signal return crosstalk is a particular problem when unbalanced signals are sent over cables between boards where the return impedance is comparable to the signal impedance [15]. Signal return crosstalk is an on-chip factor, where it takes the form of substrate current and additional IZ drops across the power distribution network. Signals can also affect one another through a shared power supply.

2.3 Transmitter- and Receiver Offsets

Transmitter- and receiver offsets occurs when the device parameter variations causes the transmitted signal level and receiver threshold to differ from their nominal values. Parameter mismatch in the transmitter may lead to the transmitted voltage differing from the ideal voltage by a transmitter offset, $V_T = V_S + V_{xo}$ [6]. Similarly, imperfections in the receiver may lead to an input offset in the detected voltage, $V_{det} = V_R + V_{ro}$. These noise sources tend to be fixed. The transmitter offsets are usually proportional to signal swings, whereas the receiver offsets are usually independent of signal swing.

3 Signaling Conventions

Transmitting digital information from one location to another and to provide a signal isolation from noise sources are key issues in a digital system design [3, 12]. Another major aspect is to provide accurate transmitter and receiver references for the signaling system. Hence, noise in either one of the references corrupts directly the signal. Therefore current-mode signaling is preferred over the voltage-mode convention, since it is difficult to provide an accurate voltage references that are isolated from the power supply noise for the small signal swings used in efficient signaling systems [6, 12].

3.1 Voltage- and Current-Mode Transmission

The current-mode transmitter, shown in Figure 1, consists of a current source that injects current $I_T(t)$ into a transmission line with impedance Z_0 [6]. Different levels of a current can be used to represent the transmitted message, usually '1' and '0'. A forward traveling wave is induced by this current to the transmission line with the amplitude:

$$V(t,x) = I_t(t - \frac{x}{v})Z_0 \tag{2}$$

Current mode transmitters provide isolation for both the signal and current return from the local power supplies. Hence, these transmitters typically have a large Z_{GT} due to the parasitic supply coupling, which provides a good isolation of signals from single supply power supply noise.

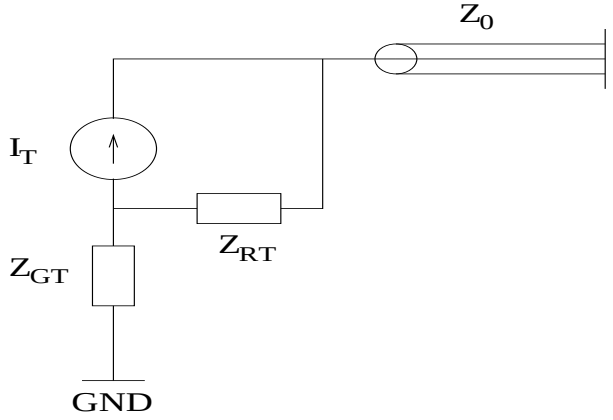

Figure 1: Current-Mode Transmitter.

Voltage-mode transmitter, shown in Figure 2, directly forces the voltage $V_T(t)$ into the transmission line. This voltage induces forward traveling wave in the line [6]:

$$V(t,x) = V_t(\frac{t-x}{v}) \tag{3}$$

By choosing $V_T = I_T Z_0$, we can generate the exactly same traveling wave as in current mode signaling. These two signaling convention differ, however, in their output impedance and their coupling to a local power supply. In reality, transmitters with output impedance much less than Z_0 considered as voltage mode transmitters and that with output impedance much greater than Z_0 as current-mode transmitters.

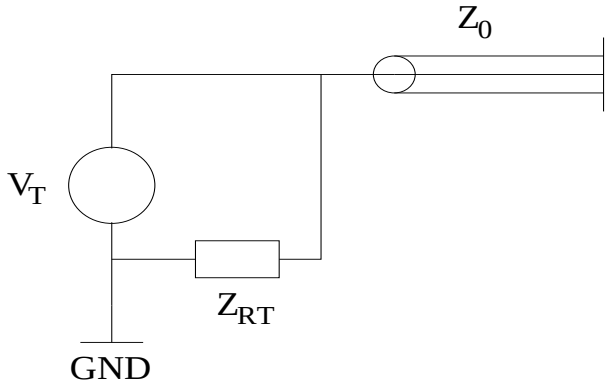

Figure 2: Voltage-Mode Transmitter.

4 Differential Signaling

A binary signal can be transmitted differentially over a pair of conductors by driving one conductor with the signal, and the other one with the complement of the signal. Differential signaling requires more pins and wires than does the single-ended signaling, namely from 1.3 to 1.8 times as many pins [6]. However, in differential signaling, the transmitter reference are less critical, since the receiver compares two voltage levels rather than comparing a voltage to a fixed reference [12]. Furthermore, the difference in relative voltage swing between '1' and '0' is twice as much compared to single-ended signaling. Therefore the doubling effect of the signal swing gives larger noise margin and a speed advantage [3].

4.1 Current-Mode Differential Signaling

The current mode signaling system, shown in Figure 3, is equivalent to provide a separate return for each signal [3]. The lines are terminated with each

other with a termination resistor $R_T = Z_0$. Therefore, when one wants to send '1', the current I_1 is injected into upper transmission line and $I_0 = -I_1$ into the lower one. Hence, the equal and opposite return currents flow in the two line's returns, which are tied to together at the ends [6].

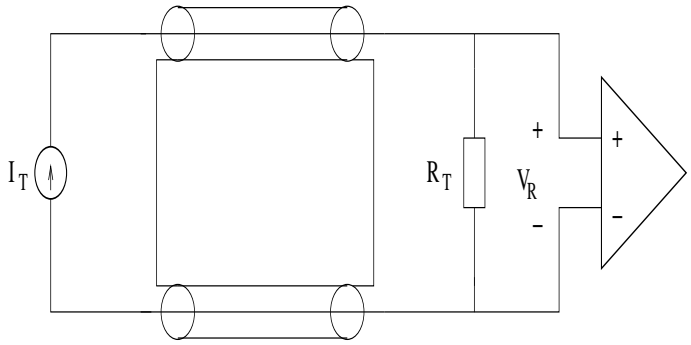

Figure 3: Differential Bipolar Current-Mode Signaling.

4.1.1 Transmitter

For differential current-mode signaling, two different transmitters are implemented. One is for the transmission line model from Spectre and the other is for RC lumped model interconnect. In a both transmitters, a source-coupled pair is used to steer the current from a current source into one of the two legs. This gives several advantages, firstly it gives an extremely sharp transient response because, depending on device sizing, the current switches from 0 to k_{Iref} over about one half of input swing, where k is the device size ratio. Secondly, the circuit draws constant current from the supply, reducing the AC component of power supply noise. Finally, the source voltage, V_S, is stable which reduces the turn-on transient, that results with the switched current-source configuration. The switch device turns on and draws current from the line to charge up the capacitance of its source node. The current-steering driver is suited to drive a balanced differential signal. The complementary outputs of the driver are attached to the two conductors of the line.

Bipolar current mode driver is designed for the transmission line model from Spectre. In this driver the two logic levels are denoted by equal amounts of current flowing in opposite directions. When this transmitter is used with the RC model it is unable to drive it, especially when the length of the transmission line is increased. Since it will have $2R + 2Z_O$ resistance in series, and R is increasing when the length of transmission line is increased.

The transmitter suitable for lumped RC-line has a source coupled current steering driver with a small resistive load, which is used to decrease the

voltage swing on the line. A simple current mirror is used for biasing the source coupled pair. Since the driver has a small load, the voltage swing on the line is small and this has advantage of increasing speed and reducing power dissipation of the interconnect. The overall signaling circuit used for the lumped RC-model transmission line is shown in the Figure 5.

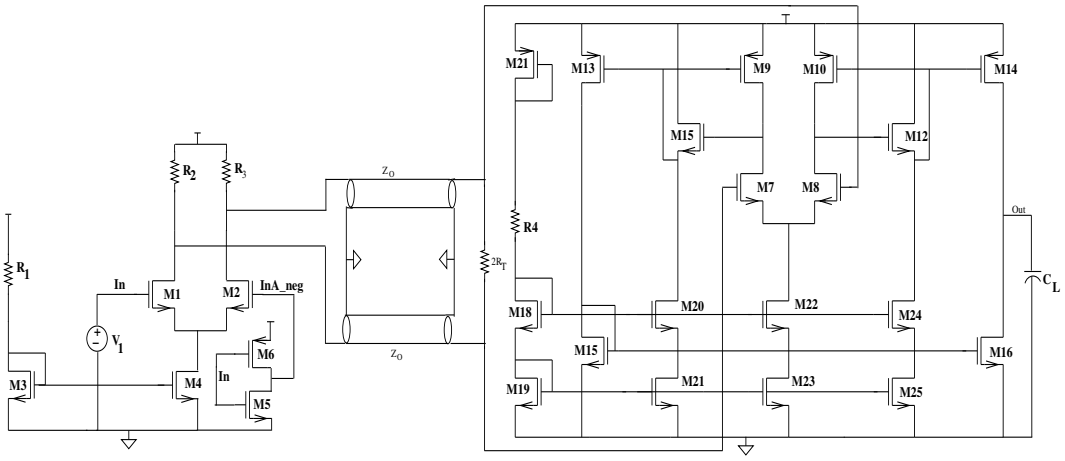

Figure 4: Differential Current-Mode Circuit Using Spectre Transmission Line Model.

4.1.2 Receiver

As in the transmitter case, two types of receivers is used. The receiver used for the Spectre model of transmission line is fully complementary and self-biased through negative feedback [2]. It has a large common mode range, for its bias condition adjusts itself to accommodate the input swing.

The receiver used for the lumped RC-model, is a single-stage class-AB differential amplifier, which consists of a NMOS source-coupled differential pair biased by a cascode current sink, illustrated in Figure 5. The cascode current sink has a relatively high output impedance and is used to achieve high input common mode rejection. The current through each load device of the differential pair is folded through current mirrors to V_{OUT}. If the gates and drains of the PMOS load devices were connected in a simple current mirror configuration, the input common-mode range of the amplifier would be limited. To reduce the power dissipation on the interconnect and to get a better speed, the voltage swing in the interconnect is small. And the load of the source coupled transmitter is small, so the common mode input from the transmitter is high, near V_{dd} , this limits the V_{ds} voltage available to the

NMOS input devices to maintain saturation. To tackle this problem, source followers (M11-M12) are used as level shifters in the PMOS current mirrors. This allows the amplifiers input common-mode range to include V_{dd}. The sizes of transistors, resistors, and capacitor are given in Appendix A, Tables 5 and 6.

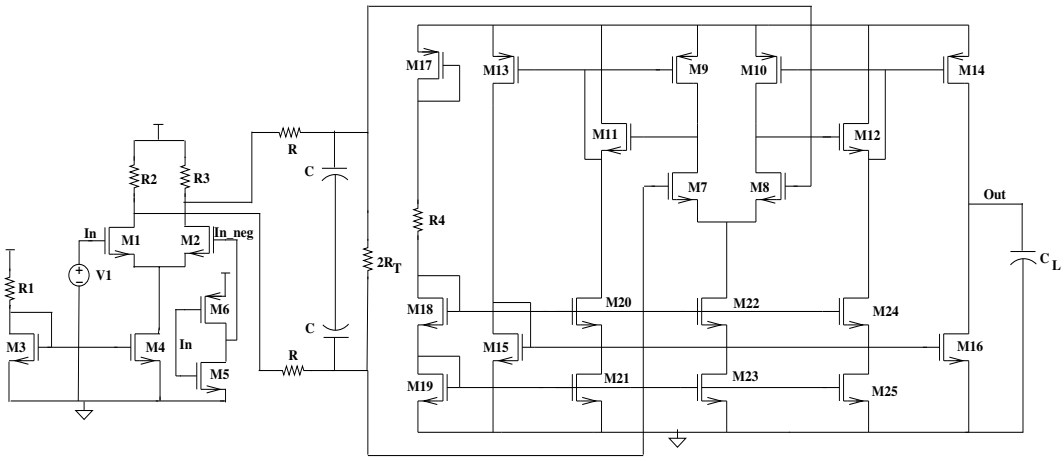

Figure 5: Differential Current-Mode Circuit Using Lumped RC-Model.

4.2 Voltage-Mode Differential Signaling

The structure of the voltage-mode signaling system is shown in Figure 6. To send a '1', the upper voltage source drives V_a to the transmission line, and the lower voltage source drives V_b on the lower transmission line. Hence, to send a '0' the voltages are reversed.

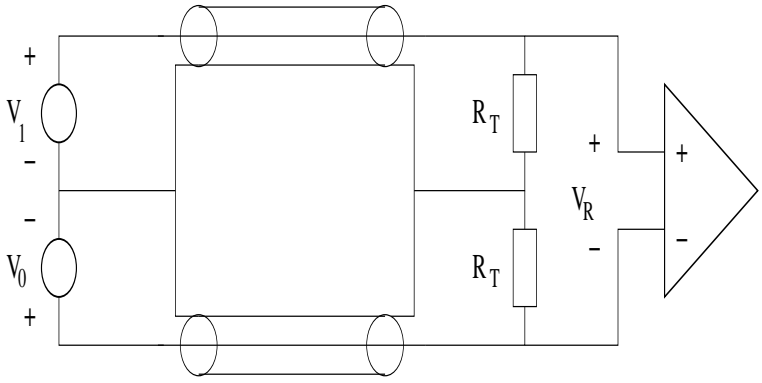

Figure 6: Voltage-Mode Differential Signaling.

4.2.1 Transmitter

Differential signaling is more immune to noise due to its high common-mode rejection, allowing for a further reduction in the signal swing. The driver is designed to drive V_1 on the upper transmission line and V_0 on the lower transmission line when it is sending '1' and vise versa to send '0'. This transmitter has very low voltage swing and is energy efficient. It uses NMOS transistor for both pull-up and pull-down [19]. The transmitter is illustrated in Figure 7 and the transistor sizes can be found in Table 4.

4.2.2 Receiver

The receiver is designed from two folded-cascode differential amplifiers, each of which are complement of the other [2]. These folded-cascode amplifiers have greater dynamic ranges than the ordinary differential amplifiers as a result of the larger drain-source voltage drop on the input pairs. This larger voltage drop maintains the input pair in the active region even for very large voltage swings of the input signal. While neither of the folded-cascode amplifier has the capability by itself to cover the entire input range, the combination of the two amplifiers can cover any range of the input. The schematic of the receiver is shown in Figure 7.

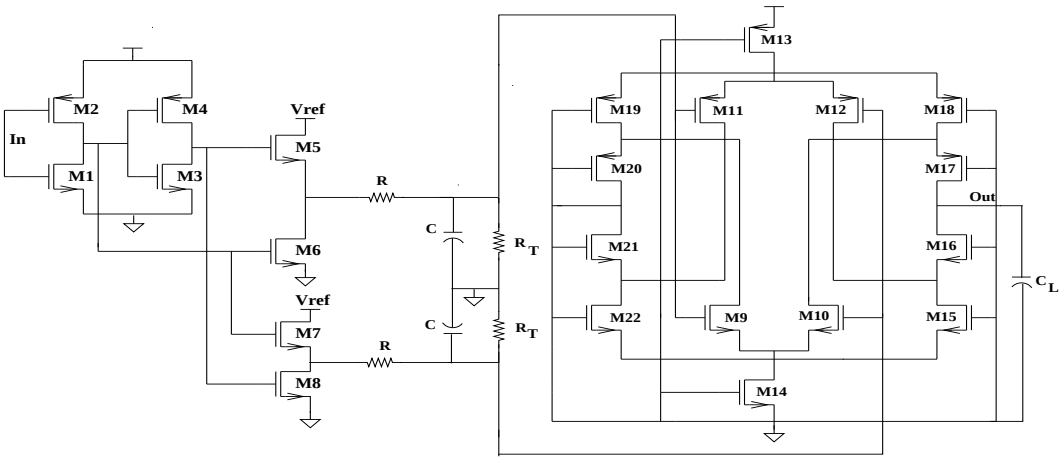

Figure 7: Voltage-Mode Differential Signaling Using Lumped RC-Model.

5 Bidirectional Signaling

The simultaneous information transfer in both directions over the transmission line has long been used in telephony. In ULSI design the effective wire density and pin count of the system can be doubled by sending bits simultaneously in both directions [7].

5.1 Current-Mode Bidirectional Signaling

Figure 8 shows a single-ended, current mode, bidirectional signaling system [6, 10]. In the transceiver A, the upper driver generates a forward current I_f, which divides equally between the terminator Z_0 and the line. The amount of the forward current I_f, that enters the line, causes a forward traveling wave with an amplitude $V_f = I_f Z_0/2$. Similarly, the reverse traveling wave is injected from the transceiver B and it has an amplitude of $V_r = I_r Z_0/2$. The voltage at position x on the line is defined as follows [6].

$$V_L(t,x) = V_f(t - \frac{x}{v}) + V_r(t - \frac{l-x}{v}) \tag{4}$$

In particular, the voltage at the two ends of the line are

$$V_{LA}(t) = V_f(t) - V_r(t - \frac{l}{v}) \tag{5}$$

$$V_{LB}(t) = V_r(t) - V_f(t - \frac{l}{v}) \tag{6}$$

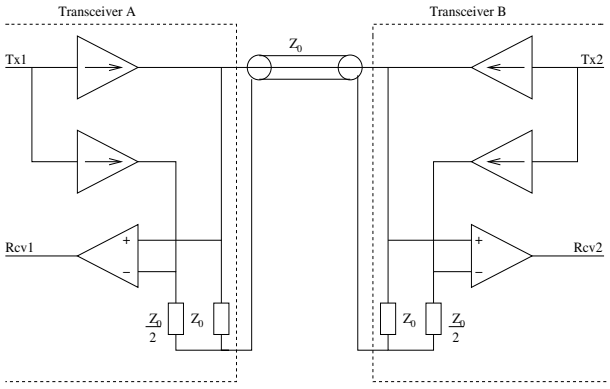

Figure 8: Current-Mode Bidirectional Signaling System.

The lower driver at the transceiver A generates a replica of the forward traveling wave. This driver generates a current, I_{f1}, that matches the current

from the top driver. The current I_{f1} is driven to the resistance $Z_0/2$, that matches the combined line-terminator seen by the upper driver [6].

Current-mode signaling provides added immunity to both power supply noise and crosstalk [13]. However this requires that the line is terminated at both ends. Induced crosstalk is reduced due to the low voltage swings which are typically associated with current-mode signaling. Furthermore, the current signal is designed to be independent of supply voltages in order to suppress power supply noise.

5.2 Transmitter

The transmitter for simultaneous bidirectional signaling is designed to drive a current signal onto a transmission line and an identical current signal through a dummy load. To accomplish this, two identical source-coupled differential pairs are used. Figure 9 shows the transmitter with both source coupled pairs. The two source-coupled pairs differ only by the load on one side. M2 is loaded with a 50 Ω resistor, which serves as the termination for the transmission line. When AC signal is applied, current flows through the transmission line and the shunt termination resistors at the opposite ends of the line are parallel. Consequently, a 25 Ω AC load is seen by M2 and a balanced source-coupled pair is achieved. At DC this is not the case, because of the negligible current flows in the transmission line and M2 sees only a 50 Ω load. This causes an offset error in the voltage applied to the receiver amplifier. An additional current sink M7 is added to null the offset error at the negative input terminal of the receiver amplifier. This additional current sink does not hinder normal operation. M7 has a relatively high output impedance; therefore when an AC signal is applied, device M3 still sees a 25 Ω load. The small resistance values of the load elements cause the DC output voltage of the transmitter to be near V_{dd}.

5.3 Receiver

The receiver, shown in Figure 10, is a single-stage class-AB differential amplifier. The amplifier consists of a NMOS source-coupled differential pair biased by a cascode current sink. The cascode current sink has a relatively high output impedance and is used to achieve high input common mode rejection. The current through each load device of the differential pair is folded through current mirrors to V_{OUT} . If the gates and drains of the PMOS load devices were connected in a simple current mirror configuration, the input common-mode range of the amplifier would be limited. The common-mode input from the transmitter is high, near V_{dd}, limiting the V_{DS} voltage available to the

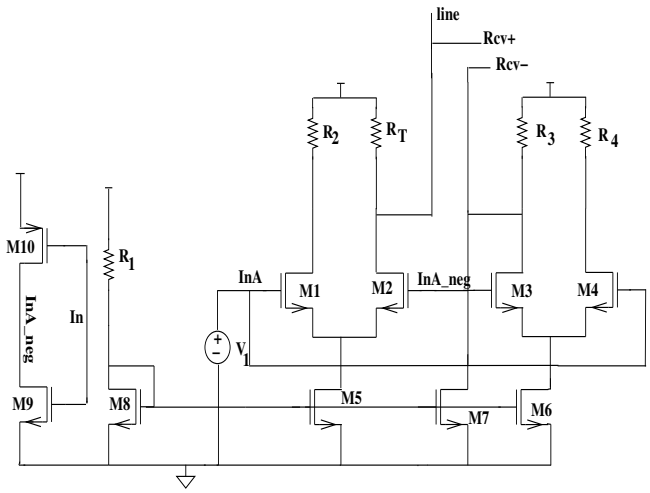

Figure 9: Transmitter Circuit for Bidirectional Current-Mode Signaling.

NMOS input devices M1 and M2 to maintain saturation. To maintain the saturation operation for M1 - M2, source followers M11 - M12 are used as level shifters in the PMOS current mirrors. This allows the amplifiers input common mode range to include V_{dd}.

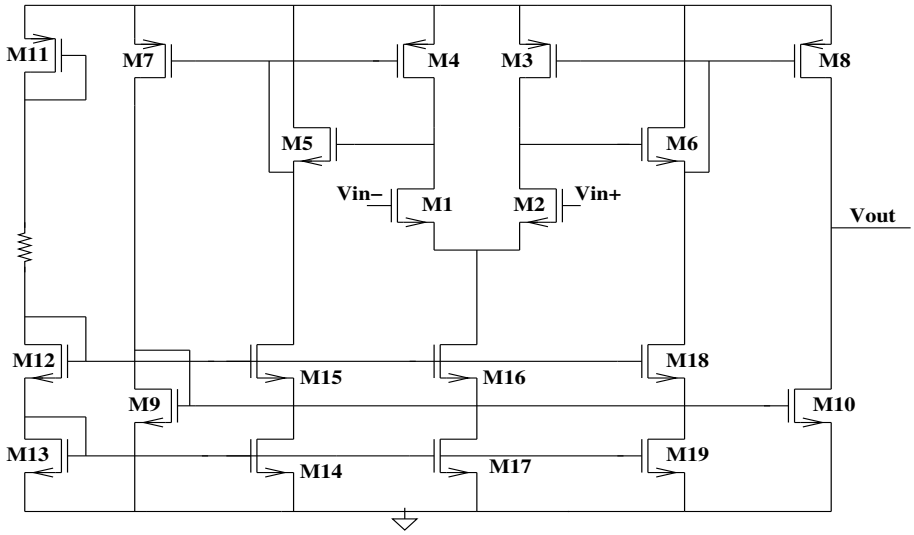

Figure 10: Receiver Circuit for Bidirectional Current-Mode Signaling.

5.4 Voltage-Mode Bidirectional Signaling

A voltage-mode bidirectional signaling system is illustrated in Figure 11. Transceiver A uses voltage-mode driver to generate generate forward signal V_{fx}, this signal is coupled to the transmission line using a series termination R_T, which halves the magnitude of the transmitted wave $V_f = \frac{V_{fx}}{2}$ [6]. A similar voltage-mode driver, V_{fx1}, generates an estimate of this voltage along with a resistive voltage divider. This estimated forward wave is subtracted by the differential amplifier from the line voltage to recover the reverse-traveling signal.

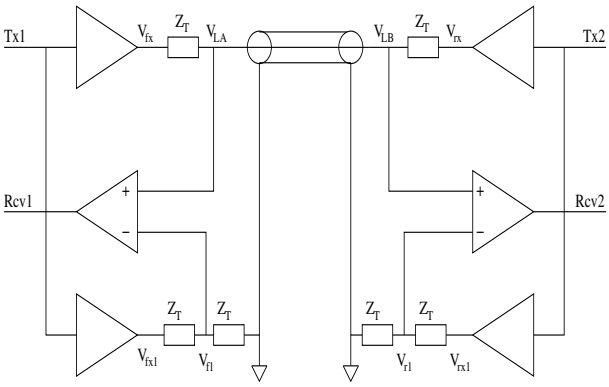

Figure 11: Voltage-Mode Bidirectional Signaling.

Voltage-mode signaling was not implemented since it does a poor job of isolating signals from power supply noise and attenuating signal-return crosstalk [13]. Furthermore, bidirectional voltage-mode signaling suffers from a return ground loop. Hence the signal return have to be tied to a reference supply at both ends of the line, making it alternate current path for that supply. Floating voltage sources, which are difficult to implementate, should be used to suppress the loop problem [6].

6 Performance Analysis

The presented signaling conventions were implemented using 0.18 μm technology. Two interconnect models were applied for the performance analysis: Lumped RC-Model and the transmission line model from Spectre. The per unit values for lumped RC-line are calculated from the technology data sheets.

6.1 Transmission Line Model

The transmitter/receiver pairs were simulated using Spectre transmission line model. The results are shown in Table 1. Transmission line component has an inherent delay of 2 ns.

Table 1: Simulation Results Using Spectre Transmission Line Model.

Design	Delay [ns]	Voltage Swing [mV]	Power [mW]	I_{peak} [mA]
Diff. Current	2.2	60	6.5	0.75
Diff. Voltage	2.4	374	14.1	11
Bidirect. Current	3.1	125	25	9.3

6.2 Lumped RC-Model

The transmission line is modeled as a lumped RC-line with the following parameters:

$$\begin{aligned} \mathrm{W} &= 0.44\ \mu\mathrm{m} \\ R_0 &= 0.078\ \tfrac{\Omega}{sq} \\ \mathrm{c} &= 0.13\ \tfrac{fF}{\mu m} \\ \mathrm{l} &= 0.333\ \tfrac{pH}{\mu m} \end{aligned}$$

Using equations from (7) to (10), the values of Resistance (R), capacitance (C), inductance (L) and characteristic impedance (Z_0) are calculated for transmission line which length varies from 0.1 mm to 3 mm.

$$R = R * \frac{L}{W} \tag{7}$$

$$Z_0 = \sqrt{\frac{l}{c}} \tag{8}$$

$$C = c * L \tag{9}$$

$$L = l * L \tag{10}$$

The RC-models of the transmission line for the differential signaling conventions are shown in Figure 12. The inductance effect is not considered in lumped models used [8, 9].

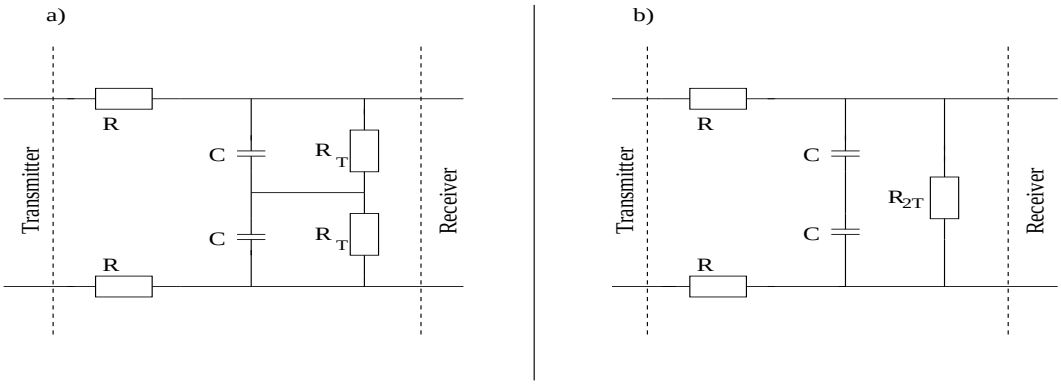

Figure 12: RC-model for the a) Voltage-Mode Differential Signaling, b)Current-Mode Differential Signaling.

6.2.1 Differential Voltage-Mode Signaling

By adopting the RC-line structure, shown in Figure 12, delay, signal swing, power consumption and peak current values were simulated for the voltage-mode differential transmitter and receiver. The delay and voltage swing are shown in Figures 13, 14 as a function of the interconnect length. Both of them are increasing along with the length of the RC-line. On the contrary the power consumption and peak-current values are decreasing when the length of the interconnect is increasing.

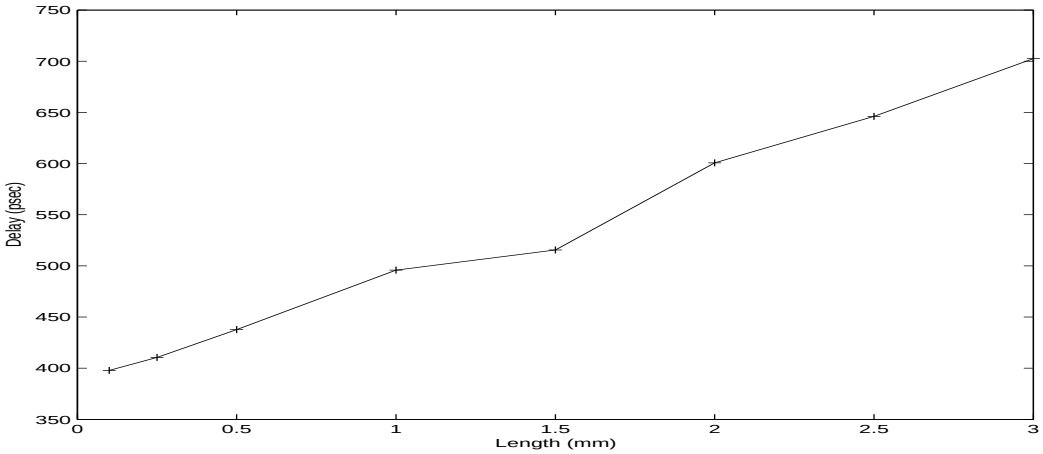

Figure 13: Delay vs. Length

The peak current values, and hence the power supply noise, decreases due to the increment in delay of the bus. Similarly the crosstalk noise can

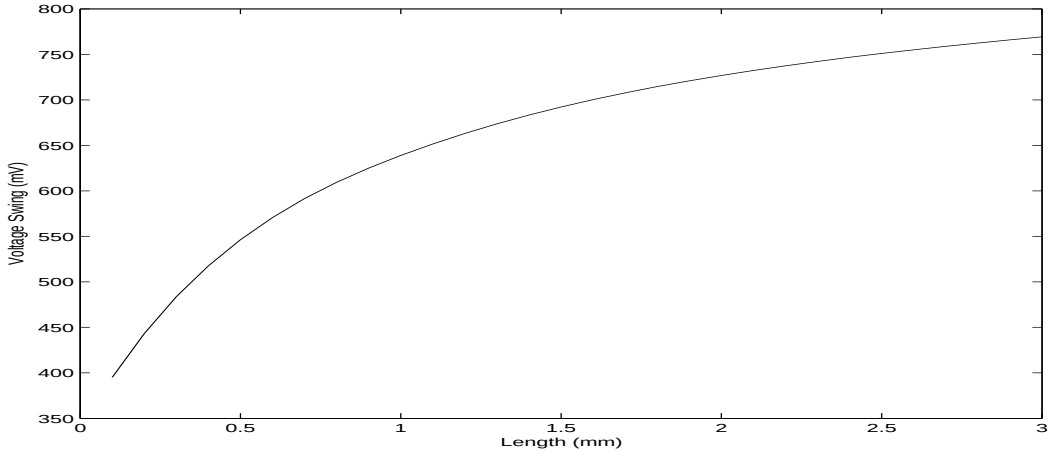

Figure 14: Voltage Swing vs. Length

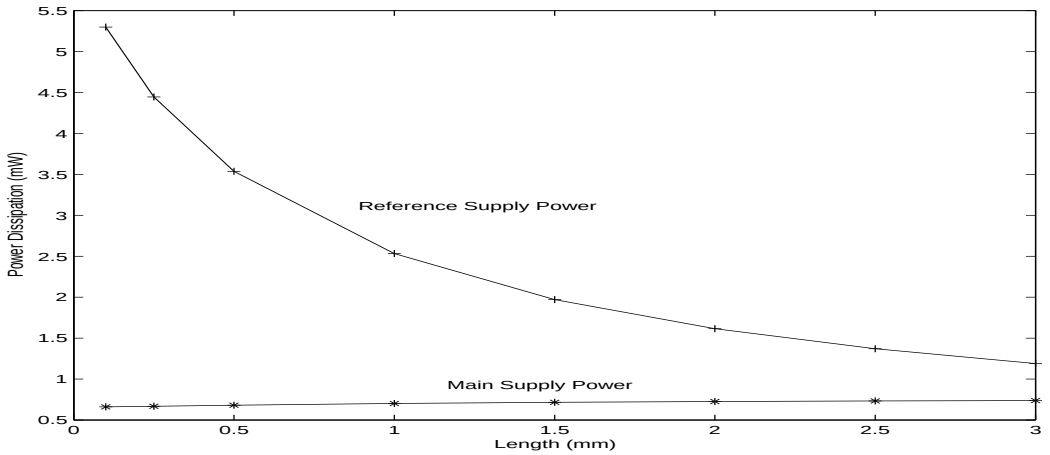

Figure 15: Peak Current vs. Length

be expected to decrease [14]. However, while the power dissipation and the peak current from the main supply are increasing, the reference values are decreasing as seen from the graphs 15,16. This is due the reference voltage of the driver, which is not able to drive the transmission line fully because of the series connected resistors ($R + R_T$), shown in Figure 12 To make the driver to drive the line, the pull up transistors width should be increased more than 100 μm, but in 0.18 μm technology the valid transistor width must be less than or equal to 100 μm. Therefore, repeaters should be inserted, if differential voltage-mode signaling is applied into long on-chip interconnects.

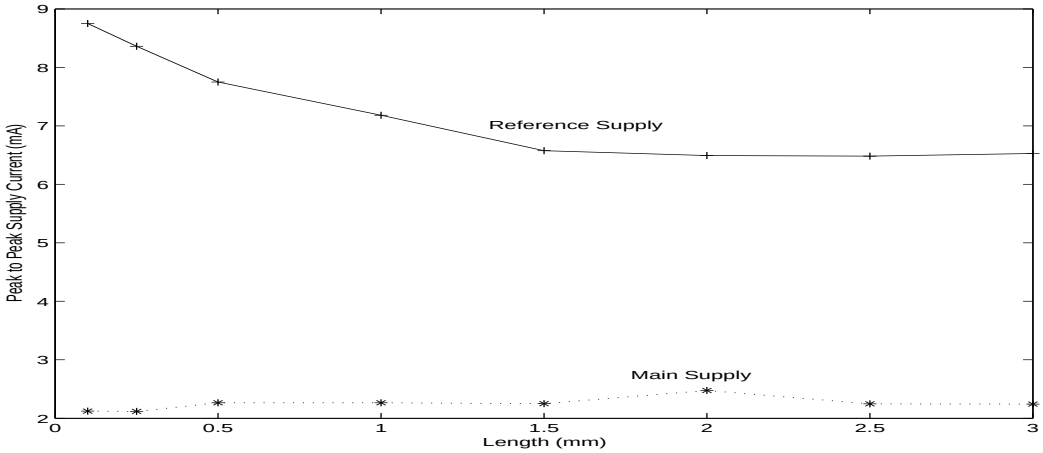

Figure 16: Power Consumption vs. Length

6.2.2 Differential Current-Mode Signaling

Utilizing the RC-line structure, shown in Figure 12, the current-mode driver and receiver pair was simulated for power consumption, voltage swing, peak current, and delay. The results are illustrated in Figures 17-20. The delay, power consumption and voltage swing of the implementation are increasing when the length of the interconnection is increasing. However, the peak current values are decreasing, due to the increment in delay. This gives potential reduction in both power supply noise and crosstalk [14, 17].

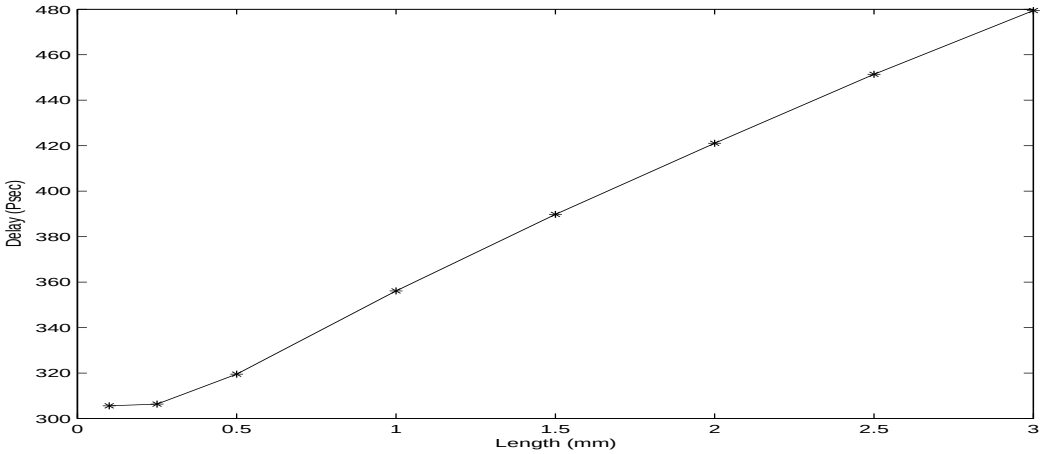

Figure 17: Delay vs. Length

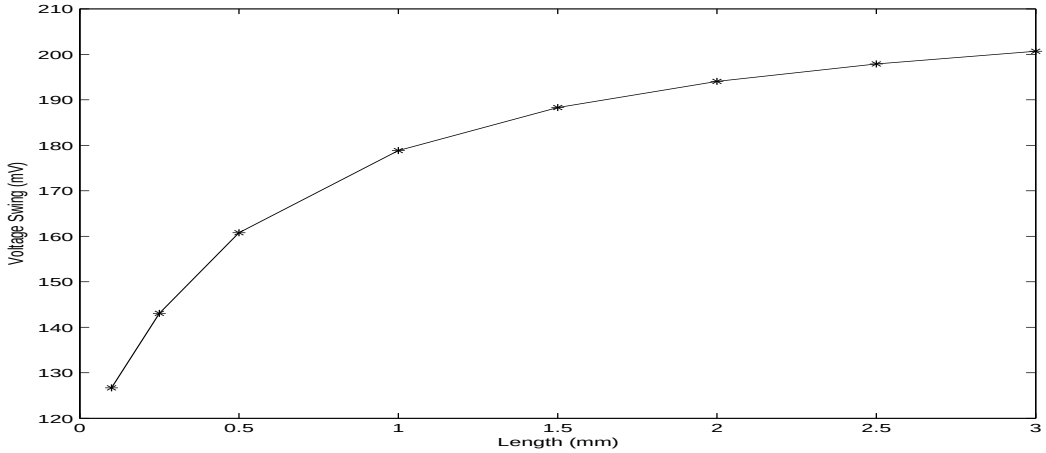

Figure 18: Voltage Swing vs. Length

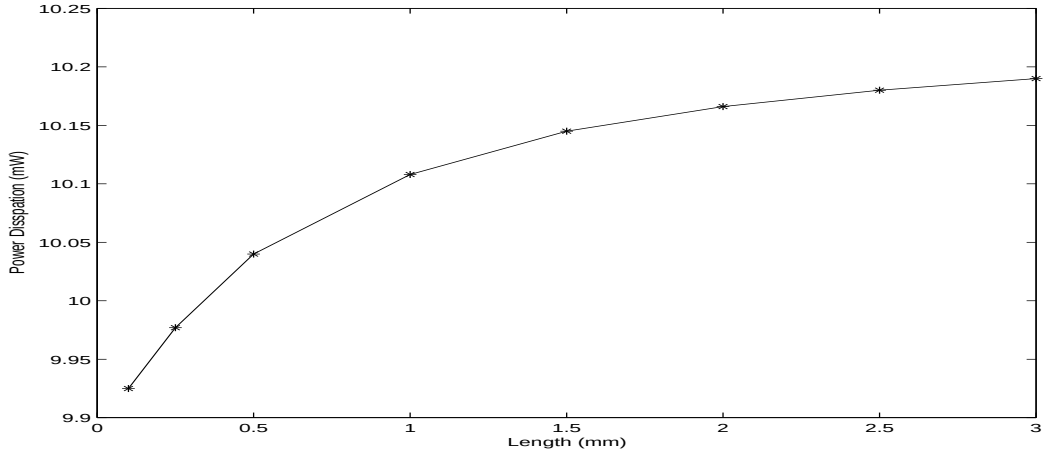

Figure 19: Power Consumption vs. Length

6.2.3 Bidirectional Signaling

The power consumption and delay of the simultaneous transmitter and receiver are increasing with the length of the interconnect as shown in Figures 21, 22. The peak current values are around a constant value of 8.2 mA. Comparing with the differential signaling conventions the peak current values are doubled. However, the small variation in I_{avg} gives potential for exploiting this signaling convention in a wide range of interconnect lengths. Furthermore, the data rate is doubled due to the bidirectional interconnect and therefore, the results are not directly comparable.

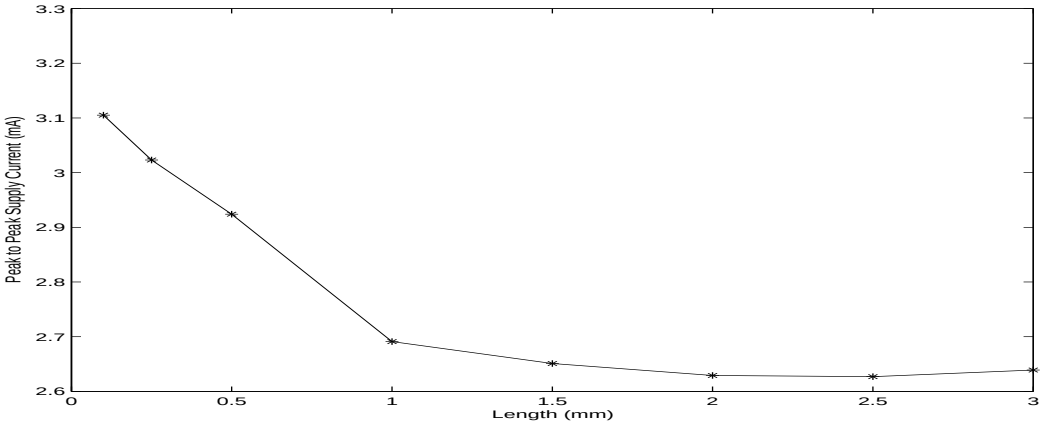

Figure 20: Peak Current vs. Length

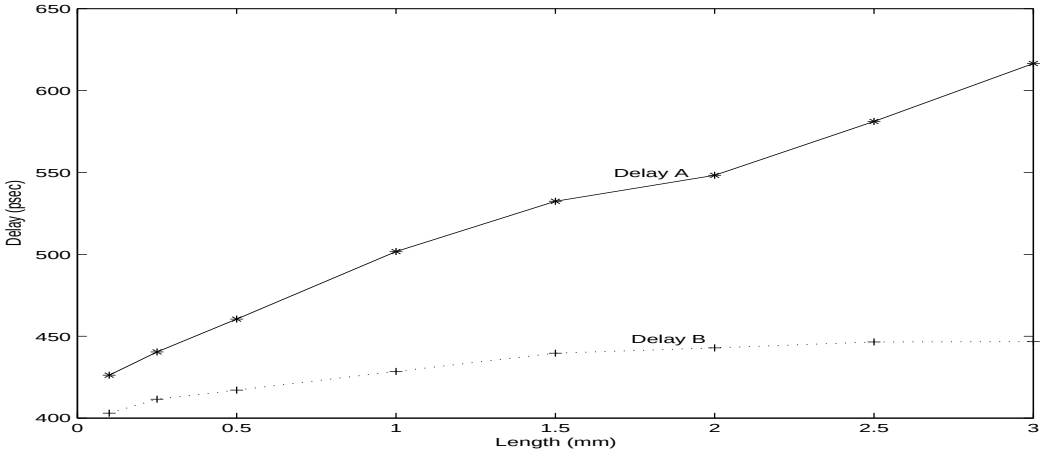

Figure 21: Delay vs. Length

6.3 Comparisons

Comparison will be made between differential current-mode and bidirectional current-mode signaling, because, as seen in Section 6.1, differential voltage-mode has inferior performance than differential current-mode signaling. Adopting the Spectre transmission line model, we can say that differential current-mode signaling has better performance but increasing pin count when compared to bidirectional signaling convention.

To exploit the RC lumped interconnect model, the delay in both signaling schemes is almost comparable. However, the power consumption is three times higher in bidirectional signaling than in the differential current-mode signaling. This increase is due to the circuit complexity in bidirectional transmitter and receiver pair. The peak current values are lower for differential

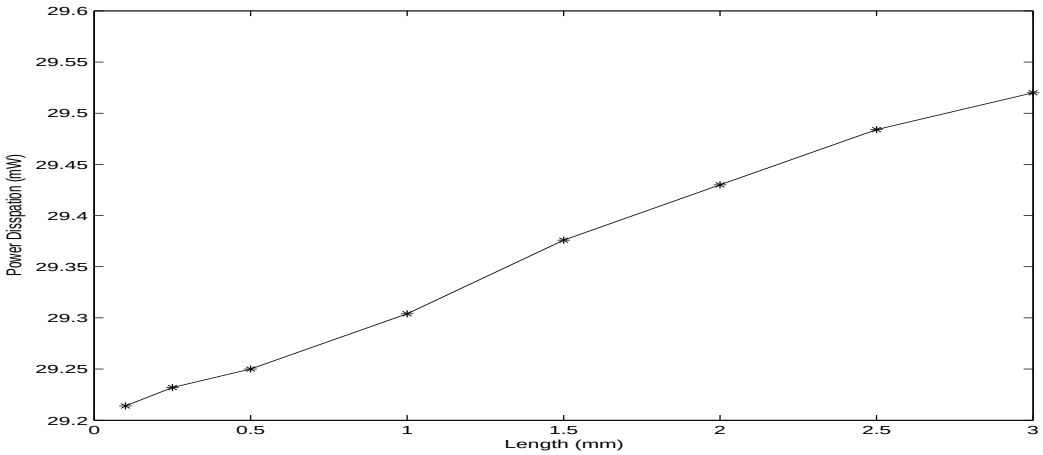

Figure 22: Power Consumption vs. Length

signaling than they are for bidirectional one. However, in the bidirectional signaling, the change in peak current values versus interconnect length is smaller in bidirectional method.

6.4 32-Bit Bus Implementation

A 32-bit wide bus structure was designed by applying the three presented signaling conventions. The interconnects were modeled using RC-model with the length of 2 mm, where the worst case switching activity is expected. The results gained from the performance analysis are shown in Table 2. From the differential signaling schemes, the current-mode bus is faster and has a smoother current profile than the voltage-mode bus.

The power dissipation of the bidirectional bus is greater than the other two differential buses, which is due to circuit complexity of the bidirectional signaling transmitters and receivers and there is also duplicate drivers from both sides of the transceivers. The power consumption in voltage-mode signaling is not as high as was expected due to following arguments (*): Firstly, the receiver used for the current-mode has more devices than voltage-mode. Secondly, the voltage-mode is not driving the line fully as explained in Section 6.2.1.

The results indicates that both of the current-mode signaling conventions have smaller delay and lower peak current values than the voltage-mode one. The bidirectional signaling has improved in performance compared to the single driver/receiver implementation. However, the pin count is doubled when comparing differential signaling over bidirectional one.

The influence of switching pattern to interconnect delay for 32-bus is pre-

Table 2: Simulation Results for 32-Bit Bus.

Design	Delay [ps]	Power [mW]	I_{peak} [mA]
Diff. Current	468	325	201
Diff. Voltage	623	75*	450
Bidirect. Current	455 (A) 409 (B)	938	298

sented in Table 3. By utililizing differential signaling conventios the worst delay results when the three wires are switching in the same direction. This shows that the differential signaling, especially current-mode implementation, has ability to provide good noise immunity and speed [15].

Table 3: The influence of switching patterns to interconnect delay.

	Diff. Voltage	Diff. Current	Bidirect. Current	
Pattern	Delay	Delay	Delay A [ps]	Delay B [ps]
↑ ↑ ↑	468	645	455	409
↑ - ↓	457	623	540	472
↑ ↓ ↑	445	606	613	548

7 Conclusion

Three signaling techniques were presented for NoC interconnects. Performance analysis were applied to these designs for speed, power consumption and noise. The interconnect is modeled using lumped RC-transmission line model and a transmission line model from Spectre. For the performance analysis, the length of the RC-line varies from 0.1 mm to 3 mm. After the separate analysis, a 32-bit bus is constructed from the implemented signaling conventions.

Differential transmitter and receiver were implemented in both current- and voltage-mode signaling conventions. Since the differential signaling has the advantage to cancel crosstalk, only power supply noise is considered. The current-mode differential signaling convention has several advantages over the corresponding voltage-mode one. Smaller voltage swing and lower peak current values provides better immunity to the power supply noise.

Simultaneous bidirectional signaling has potential to double the effective pin count and wire density in ULSI systems by sending bits simultaneously in both directions. Simultaneous transmitter/receiver was implemented with

current-mode signaling due to its superior performance over the voltage-mode bidirectional implementation. If the transmission line terminated in both ends, the current-mode implementation provides added immunity for both power supply noise and crosstalk.

Comparisons between differential current-mode signaling and bidirectional one shows that, differential current mode dissipates less power, has higher immunity and has comparable or better delay than bidirectional signaling. However, applying bidirectional signaling reduces the amount of interconnects, since the transmitter sends two signals through one interconnect. The variation in power dissipation and delay between these two signaling conventions is not that much pronounced when the length of the interconnect changes. Therefore it seems that the power consumption and delay is not as dependent of the interconnect length as in traditional signaling.

Finally, a 32-bit bus was constructed using these three signaling methods. Observe that the results are now comparable due the equal bit rates. Both current-mode signaling conventions reveals the possibility for better noise immunity and faster data transmission when compared to the voltage-mode signaling.

8 Appendix A

8.1 Differential Voltage-Mode Signaling Circuit

Assumptions : Transistors M5-M8 should be in triode region, that is,

$$V_{DS} < V_{GS} - V_{tn} \tag{11}$$

$$I_{DS} = kn'(W/L)((V_{GS} - V_{tn})V_{DS} - /fracV_{DS}2) \tag{12}$$

M9-M12 are in saturation, that is

$$V_{DS} > V_{GS} - V_{tn} \tag{13}$$

$$I_{DS1} = I_{DS2} = kn'(W/L)(V_{GS} - V_{tn})2 \tag{14}$$

The Bias current of the receiver circuit is adjusting itself according to the input through negative feedback. This feature has the advantage of having stabilized bias. The above Equations are taken from [16].

Table 4: Transistor Sizes for Differential Voltage-Mode Circuit.

Transistor M_i	Width [μm]	Length [μm]
M1	5	0.18
M2	12	0.18
M3	5	0.18
M4	12	0.18
M5	20	0.18
M6	15	0.18
M7	20	0.18
M8	15	0.18
M9	5	0.18
M10	5	0.18
M11	13	0.18
M12	13	0.18
M13	5	0.18
M14	3	0.18
M15	7	0.18
M16	3	0.18
M17	3	0.18
M18	7	0.18
M19	4	0.18
M20	0.44	0.18
M21	0.44	0.18
M22	4	0.18
R_T	50 Ω	
C_T	10 fF	

8.2 Current-Mode Signaling Circuits

A simple current-mirror is used as a current source in the Bipolar current driver. Let the current through M8, diode connected NMOS transistor be I_1, then the bias current through M5, $I_{biasn} = /fracW_5W_8I_1$. This bias current should be equal with the bias current from the PMOS diode connected one, that is, the current through M6, $I_{biasp} = \frac{W_6}{W_7}I_2$, where I_2 is the current through M7. Transistors M5-M8 should be in saturation to act as a proper current mirror [6]. Both the source-coupled pairs of NMOS and PMOS transistors are also in saturation. When we come to the receiver circuit, the two bias voltages of M15 and M16 connected each other to the internal amplifier node V_{BIAS}. This self-biasing of the amplifier creates a negative-feedback loop that stabilizes the bias voltages. Transistors M15-M16 operates in their linear region and transistors M11-M14 operates in saturation region.

Source-coupled current steering driver is used as a driver in this signaling. Simple current mirror is used as a current sink for the driver. As explained in the above section, current mirror transistors, M3-M4, and source-coupled transistors, M1-M2, are in saturation region . In the receiver circuit, cascode current mirror is used as a current-sink because it has high output impedance [11]. This has an advantage to achieve high input common-mode rejection. Transistors M18-M25 of the cascode mirror and the source coupled M7-M8 are in the active region.

8.3 Simultaneous Bidirectional Signaling Circuits

In the bidirectional signaling, two identical drivers are needed, one is to drive the line and the other is to duplicate the driver output used for recovering the opposite end input. Both these drivers are source-coupled current steering driver. Simple current mirror is used as a current-sink. Transistor M7, to null the offset error at the negative input of the receiver. M7 has high output impedance. All the transistors are in active mode. The receiver circuit are the same as the differential current-mode receiver circuit used for the lumped RC model.

Table 5: Transistor Sizes for Differential Current-Mode Circuit Using Spectre Transmission Line Model.

Transistor M_i	Width [μm]	Length [μm]
M1	8	0.18
M2	8	0.18
M3	20	0.18
M4	20	0.18
M5	7	0.18
M6	20	0.18
M7	2	0.18
M8	0.44	0.18
M9	5	0.18
M10	12	0.18
M11	3	0.18
M12	3	0.18
M13	5	0.18
M14	5	0.18
M15	9	0.18
M16	8	0.18
R1,R2	25 Ω	
R_T	50 Ω	
C_T	10 fF	

Table 6: Transistor Sizes for Differential Current-Mode Circuit Using Lumped RC-Model.

Transistor M_i	Width [μm]	Length [μm]
M1	10	0.18
M2	10	0.18
M3	0.24	0.18
M4	15	0.18
M5	5	0.18
M6	12	0.18
M7	20	0.18
M8	20	0.18
M9	3.6	0.54
M10	3.6	0.54
M11	5.59	0.18
M12	5.59	0.18
M13	2	0.18
M14	20	0.42
M15	1.8	0.18
M16	7.27	0.235
M17	11.962	0.18
M18	1	0.18
M19	0.24	0.18
M20	6.257	0.18
M21	5.316	0.18
M22	6.257	0.18
M23	5.316	0.18
M24	6.257	0.18
M25	5.316	0.18
R1,R4	25 Ω	
R2,R3	50 Ω	
R_T	102 Ω	
C_T	10 fF	

Table 7: Transistor Sizes for Simultaneous Bidirectional Signaling Using Spectre Transmission Line Model

Transistor M_i	Width [μm]	Length [μm]
M1	8.497	0.18
M2	8.497	0.18
M3	8.497	0.18
M4	8.497	0.18
M5	5.704	0.18
M6	5.704	0.18
M7	0.5	0.45
M8	1.704	0.18
M9	5	0.18
M10	12	0.18
M11	20	0.18
M12	20	0.18
M13	3.6	0.54
M14	3.6	0.54
M15	10.589	0.18
M16	10.589	0.18
M17	2	0.18
M18	20	0.49
M19	1.8	0.18
M20	6.27	0.27
M21	11.962	0.18
M22	0.44	0.18
M23	0.24	0.18
M24	6.257	0.18
M25	5.316	0.18
M26	6.257	0.18
M27	5.316	0.18
M28	6.257	0.18
M29	5.316	0.18
R1,R2,R3,R4	25 Ω	
R_T	50 Ω	
C_T	10 fF	

Table 8: Transistor Sizes for Simultaneous Bidirectional Signaling Using Lumped RC-Model

Transistor M_i	Width [μm]	Length [μm]
M1	8.497	0.18
M2	8.497	0.18
M3	9.497	0.18
M4	9.497	0.18
M5	5.704	0.18
M6	8.704	0.18
M7	2	0.45
M8	1.704	0.18
M9	5	0.18
M10	12	0.18
M11	20	0.18
M12	20	0.18
M13	3.6	0.54
M14	3.6	0.54
M15	10.589	0.18
M16	10.589	0.18
M17	2	0.18
M18	20	0.49
M19	1.8	0.18
M20	6.27	0.27
M21	11.962	0.18
M22	0.44	0.18
M23	0.24	0.18
M24	6.257	0.18
M25	5.316	0.18
M26	6.257	0.18
M27	5.316	0.18
M28	6.257	0.18
M29	5.316	0.18
R1,R2,R3,R4	25 Ω	
R_T	50 Ω, 100 Ω, 200 Ω, 250 Ω	
C_T	10 fF	

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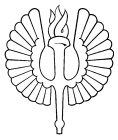

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