Power Distribution TSVs induced Core Switching Noise

Waqar Ahmad[1], Rajeev Kumar Kanth[2], Qiang Chen[1], Li-Rong Zheng[1], and Hannu Tenhunen[1]

[1]Department of Electronics and Computer Systems, KTH Royal Institute Of Technology, Forum 120, 16440 Kista, Stockholm Sweden.
[2]Turku Centre for Computer Science (TUCS), University of Turku, Finland.
[1]{ahmadw, qiangch, lirong, hannu}@kth.se
[2]rajeev.kanth@utu.fi

***Abstract*—Size of on-chip interconnects as well as the supply voltage is reducing with each technology node whereas the operating speed is increasing in modern VLSI design. Today, the package inductance and resistance has been reduced to such an extent that core switching noise caused by on-chip inductance and on-chip resistance is gaining importance as compared to I/O drivers switching noise. Both on-chip inductance and skin effect are prime players at frequencies of the order of GHz. The problem is further aggravated when chips are interconnected through TSVs to form a 3D integrated stack in order to achieve low form factor and high integration density. In this paper we analysed peak core switching noise in a 3D stack of integrated chips interconnected through power distribution TSV pairs, through our comprehensive mathematical model which has been proved to be quite accurate as compared to SPICE. We analysed the effect of number of chips in a 3D stack, rise time, decoupling capacitance, and skin effect on power distribution TSVs induced core switching noise in this paper.**

Keywords: core switching noise, rise time, 3D stack, skin effect.

I. INTRODUCTION

Shrinking technology below *45nm* is not as much effective because of increased gate leakage and increased device delay as compared to interconnect delay. 3D integration technology is therefore, gaining more attention. Chip stacking through wire bonds doesn't guarantee good power integrity due to large equivalent series inductance [1]. State-of-the-art technology is therefore, through-silicon-via (TSV) to stack dies in vertical direction as shown by Fig. 1 [2]. 3D system in package (SiP) is a promising technology due to short interconnects and low form factor which is suitable for small and lightweight high performance mobile electronics devices [1]. Therefore, TSV nanotechnology needs accurate power integrity estimation due to tight noise margins [3].

Core switching noise has been overlooked in past because of dominant package inductance. However in modern 3D packaging high density BGAs along with TSVs and micro-connects are used instead of wire bonding. Chips are currently working at GHz internal clock frequency which is several folds than their I/O speeds [4]. Because of high speed and high integration densities in VLSI/ULSI chips, the noise caused by core logic switching has become a critical factor [4]. Moreover, the skin effect at high frequency causes IR drop. *K-tier* 3D chip has *k* times as much current as a single 2D chip of the same footprint [5]. Therefore, power delivery problem is worsened in 3D ICs due to introduction of additional TSV resistance [5].

Ldi/dt or delta-I noise can't be neglected due to high inductance of on-chip power distribution network at high frequencies. The ratio of delta-I noise to nominal supply voltage V_{dd} is given by [6]:

$$\frac{L\frac{\partial i}{\partial t}}{V_{dd}} \approx \frac{L P f_c}{V_{dd}^2} \quad (1)$$

Where:
L= on-chip inductance of power distribution network.
P= power consumed on-chip.
f_c= chip clock frequency.

Equation (1) shows that ratio of delta-I noise to V_{dd} has been increased significantly due increased integration density and clock frequency.

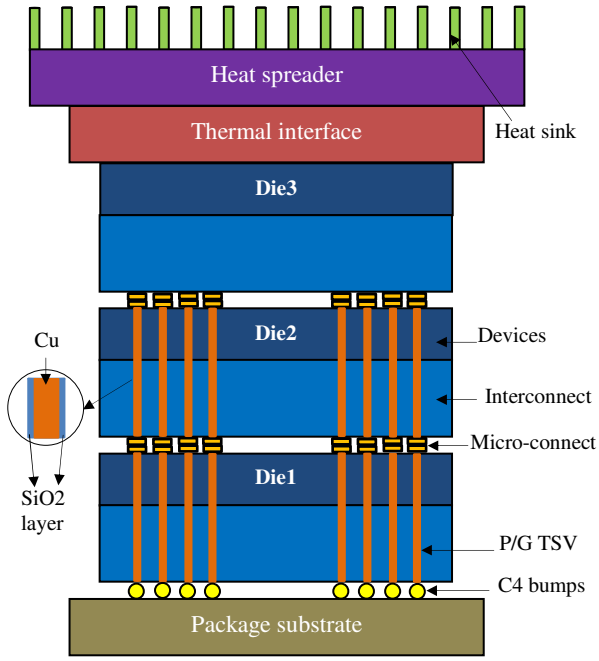

Fig. 1. Three dies forming a 3D system with face-to-back bonding through micro-connects. Power is supplied through vertical TSV pairs from package substrate.

On-chip power distribution network has to be designed to confine the voltage fluctuations within 5-10% of the nominal supply voltage V_{dd} [7]. The fluctuations in supply voltage caused by IR drop and delta-I noise may cause timing uncertainties and logic failures. Therefore, a 10% fluctuation in supply voltage may translate to a more than 10% timing uncertainty in integrated circuits [6]. That is why we analysed core switching noise induced by power distribution TSVs in this paper.

Rest of the paper is organised as follows. We discuss previous work in section II. In section III we give noise estimation model, we proposed in [8]. Section IV shows simulation setup. We discuss results in section V and draw conclusions in section VI.

II. PREVIOUS WORK

There has been significant work regarding core switching noise in 2D ICs [4] [9-10] but corresponding work in 3D ICs is quite insufficient as compared to recent boom in 3D integration technology. The effect of TSV distribution, tier number, and the location of powering on processing units has been analysed in [11] based on 3D MPSoC P/G noise simulation platform. A comprehensive study of TSV induced noise characterization in high-R and EPI substrates as a function of some critical design and process parameters like signal slew rate, TSV height, ILD thickness, and TSV-to-device and TSV-to-TSV spacing is presented in [12]. The author in [13] claims through experimental results that up to 70% voltage variation is caused by the failure of a single TSV. An analytical switching noise model has been proposed in [14] considering substrate coupling on TSVs.

III. MODEL TO ESTIMATE CORE SWITCHING NOISE

Fig. 2(a) [8] shows physical model of orthogonal global supply grids of two chips interconnected through TSVs. Fig. 2(b) [8] shows equivalent pi-model of a power distribution TSV pair. Fig. 2(c) [8] shows equivalent electrical model of two neighbouring chips interconnected through a power distribution TSV pair.

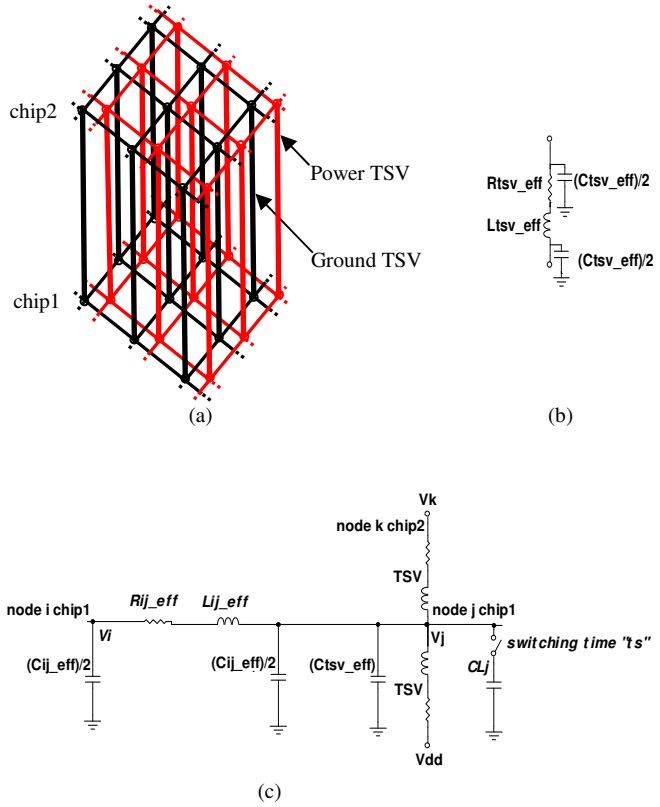

Fig. 2 (a) 3X3 orthogonal global supply grids of two neighbouring chips in a 3D stack inter-connected through TSVs where red colour indicates power grid and black colour indicates corresponding ground grid. (b) Equivalent Pi-model of power distribution TSV pair. (c) Effective RLC Model of node j on chip1 connected to node i on same chip and node k on chip2 where V_{dd} is nominal supply voltage and CL_j is switching load connected to node j with switching time t_s.

In Fig. 2(c) $R_{i,j}$, $R_{k,j}$, $L_{i,j}$, $L_{k,j}$, $C_{i,j}$ and $C_{k,j}$ are metal segments equivalent resistance, inductance and capacitance whereas C_{L_j} includes logic load equivalent capacitance, TSV capacitance and decoupling capacitance.

We have *nxn* matrix form equation from [8] where a given chip has *1* to *n* nodes and neighbouring chip connected to it through TSVs has *1* to *2n+1* nodes:

$$
\begin{bmatrix}
-1 & \frac{X_{1,2}}{\lambda_1} & \frac{X_{1,3}}{\lambda_1} & \cdots & \frac{X_{1,m}}{\lambda_1} & \cdots & \frac{X_{1,n}}{\lambda_1} \\
\frac{X_{2,1}}{\lambda_2} & -1 & \frac{X_{2,3}}{\lambda_2} & \cdots & \frac{X_{2,m}}{\lambda_m} & \cdots & \frac{X_{2,n}}{\lambda_n} \\
\vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\
\frac{X_{m,1}}{\lambda_m} & \frac{X_{m,2}}{\lambda_m} & \frac{X_{m,3}}{\lambda_m} & \cdots & -1 & \cdots & \frac{X_{m,n}}{\lambda_m} \\
\vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\
\frac{X_{n,1}}{\lambda_n} & \frac{X_{n,2}}{\lambda_n} & \frac{X_{n,3}}{\lambda_n} & \cdots & \frac{X_{n,m}}{\lambda_n} & \cdots & -1
\end{bmatrix}
\begin{bmatrix} V_1^{\min} \\ V_2^{\min} \\ \vdots \\ V_m^{\min} \\ \vdots \\ V_n^{\min} \end{bmatrix}
+
\begin{bmatrix}
\frac{X_{1,n+1}}{\lambda_1} & \frac{X_{1,n+2}}{\lambda_1} & \frac{X_{1,n+3}}{\lambda_1} & \cdots & \frac{X_{1,n+m}}{\lambda_1} & \cdots & \frac{X_{1,2n}}{\lambda_1} \\
\frac{X_{2,n+1}}{\lambda_2} & \frac{X_{2,n+2}}{\lambda_2} & \frac{X_{2,n+3}}{\lambda_2} & \cdots & \frac{X_{2,n+m}}{\lambda_2} & \cdots & \frac{X_{2,2n}}{\lambda_2} \\
\vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\
\frac{X_{m,n+1}}{\lambda_m} & \frac{X_{m,n+2}}{\lambda_m} & \cdots & \cdots & \frac{X_{m,n+m}}{\lambda_m} & \cdots & \frac{X_{m,2n}}{\lambda_m} \\
\vdots & \vdots & \vdots & \cdots & \vdots & \cdots & \vdots \\
\frac{X_{n,n+1}}{\lambda_n} & \frac{X_{n,n+2}}{\lambda_n} & \cdots & \cdots & \frac{X_{n,n+m}}{\lambda_n} & \cdots & \frac{X_{n,2n}}{\lambda_n}
\end{bmatrix}
\begin{bmatrix} V_{n+1}^{\min} \\ V_{n+2}^{\min} \\ \vdots \\ V_{n+m}^{\min} \\ \vdots \\ V_{2n}^{\min} \end{bmatrix}
$$

$$
=
\begin{bmatrix}
-\frac{1}{2\lambda_1}\left(\sum_{i=2}^{n} C_{i,1} + \sum_{k=n+1}^{2n} C_{k,1}\right) V_{dd} \\
-\frac{1}{2\lambda_2}\left(\sum_{\substack{i=1 \\ i\neq 2}}^{n} C_{i,2} + \sum_{k=n+1}^{2n} C_{k,2}\right) V_{dd} \\
\vdots \\
-\frac{1}{2\lambda_m}\left(\sum_{\substack{i=1 \\ i\neq m}}^{n} C_{i,m} + \sum_{k=n+1}^{2n} C_{k,m}\right) V_{dd} \\
\vdots \\
-\frac{1}{2\lambda_n}\left(\sum_{i=1}^{n-1} C_{i,n} + \sum_{k=n+1}^{2n} C_{k,n}\right) V_{dd}
\end{bmatrix}
\qquad (2)
$$

Where minimum switching voltages on bottom chip are $V_1^{min}....V_n^{min}$ and minimum switching voltages on top chip are $V_{n+1}^{min}....V_{2n}^{min}$. We can find minimum voltage at all the nodes of two neighbouring chips interconnected through TSVs during switching of core logic by solving equation (2). Core switching noise at any node is found by subtracting the minimum voltage at that node from nominal supply voltage V_{dd}. The formulation of equation (2) along with all other parameters is given by [8].

IV. SIMULATION SETUP DETAILS

The model is based on orthogonal and paired P/G grids as shown by Fig. 2(a) [8]. The orthogonal grid on each chip is interconnected through via at each crossing point i.e. where power line crosses the power line and ground line crosses the ground line. Global supply grids of any two neighboring chips can be interconnected through TSVs at all crossing points. The logic load is on bottom layer and there may be a number of layers between global supply grid and bottom layer on each chip, depending on chosen technology node. Assume that resistance of solder bumps, micro-connects and vias is also included in equivalent TSV resistance. Assume that supply grid including TSVs is made of Cu and substrate is made of silicon. Assume that each TSV has *0.25um* SiO2 layer around it while crossing through Si substrate in order to reduce leakage between TSVs and substrate. Assume that TSVs have aspect ratio of *10* with *30um* pitch. Assume a square supply grid with *1mm* side, *100um* pitch and *15um* spacing between each power and corresponding ground line. We use single pair of TSVs at the centre to interconnect global supply grids of two neighboring chips throughout the analysis. We followed [15] for line width, pitch, spacing, and supply grid area relationship thereby reserving *50%* of metal resources for supply on each chip. RLC values for TSVs, line segments and supply grid are found through Ansoft Q3D Extractor. We assume rise time equal to switching time of the logic load for peak switching noise induced by each TSV pair. We followed [16] to assign logic load, switching time, and decoupling capacitance associated with each TSV pair. The nominal supply voltage V_{dd} is equal to *1V* and *10%* ripple is allowed in supply voltage. We estimate the core switching noise by solving the system of equations (2) for minimum switching voltages at each node.

V. RESULTS AND DISCUSSION

The grid size is 1mmx1mm for all the figures and rest of the parameters are same as mentioned in section IV.

Fig. 3 shows a steep rise in TSVs induced core switching noise when number of dies is increased in a 3D stack.

Fig. 4 shows core switching noise in a stack of two chips interconnected through single pair of TSVs, increases by increasing the frequency. It is because of the combined effect of increase in inductance and skin effect at high frequency.

Fig. 5 shows a steep rise in the impedance of power distribution network in a stack of two chips interconnected through single pair of TSVs, beyond 6GHz frequency. It is because of both skin effect and higher inductance.

Fig. 6 shows a steep decrease in core switching in a stack of two chips interconnected through single pair of TSVs, by increasing rise time or in other words decreasing the frequency. It is because of decrease in skin effect and inductance of power distribution TSVs.

Fig. 7 shows that core switching noise decreases drastically by adding more decoupling capacitance in a stack of two chips interconnected through single pair of TSVs. This type of analysis helps the designer to optimize decoupling capacitance during initial phase of the design.

VI. CONCLUSIONS

The analysis is based on our comprehensive mathematical noise model which has been proved to be quite accurate as compared to SPICE in [8]. This analysis is helpful in early design tradeoffs to meet tight noise margins for the design of modern 3D power distribution network. The designer can choose suitable physical dimensions of TSVs/power distribution bus, clock frequency/rise time, maximum number of chips in a 3D stack, and value of decoupling capacitance to meet noise margin requirements for a particular design.

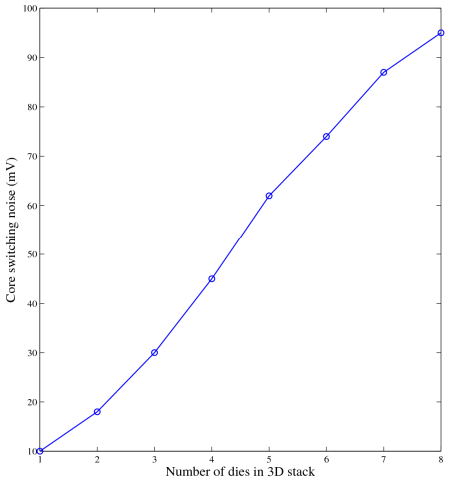

Fig. 3. Increase in core switching noise by increasing number of dies in 3D stack where neighbouring chips are interconnected through single TSV pair. Grid size is 1mmx1mm on each die. TSV height is *50um* and diameter is *5um*. Rise time is *0.5pS*.

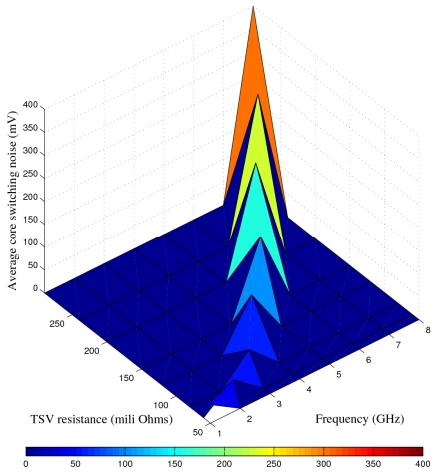

Fig. 4. Increase in core switching noise within a stack of two dies due to increase in TSV resistance due to skin effect by increasing the frequency.

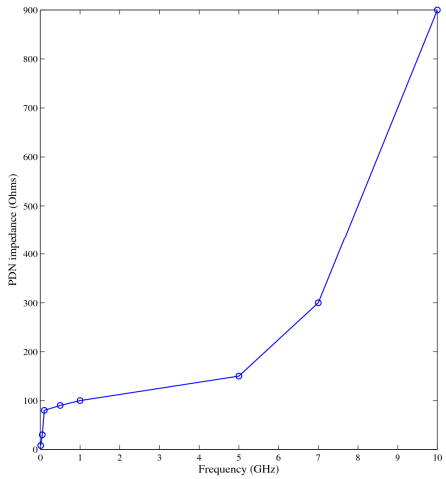

Fig. 5. Increase in the impedance of power distribution network (PDN) by increasing the frequency.

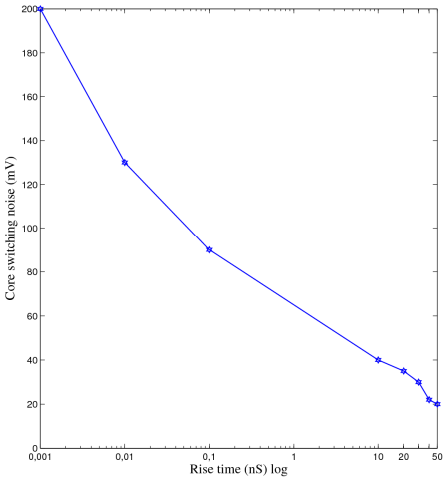

Fig. 6. Reduction in core switching noise by increasing the rise time.

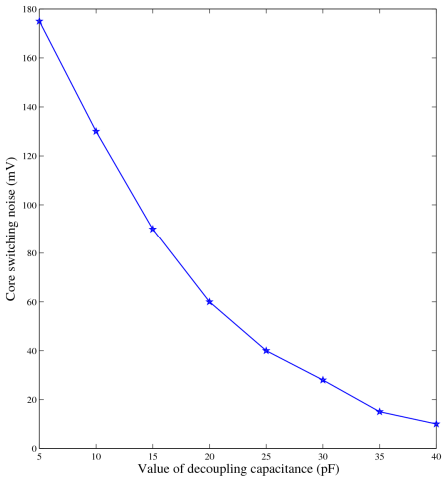

Fig. 7. Reduction in core switching noise by increasing the value of decoupling capacitance.

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