ANALYSES OF SIGNALING TECHNIQUES FOR SELF-TIMED SYSTEMS

*Ethiopia Nigussie *, Johanna Tuominen *, and Jouni Isoaho*

Communication Systems Laboratory
Dept. of Information Technology
University of Turku, Finland
{ethnig | joeltu | jisoaho}@utu.fi

ABSTRACT

This paper presents signaling techniques for global and local on-chip interconnects, namely voltage-mode and current-mode differential signaling and simultaneous bidirectional signaling. In the proposed approach, these techniques were applied along with the self-timed design methodology to the interconnects of the path metric unit of the Viterbi decoder, and to the global on-chip bus segment. The simulations are performed using 0.18 μm technology. These interconnects are compared in terms of power consumption, noise, and speed. The study considered in this paper revealed the possibilities of current-mode signaling in global on-chip interconnects, while for local interconnects, the optimal result is achieved by applying voltage-mode signaling.

1. INTRODUCTION

By looking a few years ahead, a single-chip or single-package system in 2010 will be a fault-tolerant, on-chip distributed real-time system consisting of up to a hundred resources communicating over a sophisticated communication infrastructure. Typical individual resources will be processor cores, memories, configurable logic blocks, optimized digital single-function blocks, and mixed-signal interface blocks. In modern system-on-chip (SoC) design, a significant effort has to be invested to optimization of on-chip communication links between system modules and to verification of overall functionality and timing. This is because performance, reliability, and also power consumption of the system strongly depend on the implementation of module interconnects [7].

A signaling technique involves in encoding information into current or voltage, generating a reference against which this quantity is measured, providing terminations to couple signal energy into the transmission medium and absorb energy to prevent unwanted reflections, and controlling signal transitions to limit the spectrum of transmitted energy [1]. An efficient signaling scheme is the one that maximizes the data rate per pin, minimizes power dissipation, and provides good noise immunity [4]. Such signaling convention can dramatically increase available data rate, and hence system performance.

In this paper we present two signaling conventions for SoC interconnects, current-mode differential signaling and current-mode simultaneous bidirectional signaling. These techniques were selected among the existing signaling scheme, of which has a promising feature for the future technology scaling impact. Finally, these signaling techniques were applied to the interconnects of the path metric unit of Viterbi decoder and to the global on-chip bus segment. Performance analysis was carried out for power consumption, speed and reliability using conventional voltage-mode signaling as a reference.

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2. SIGNALING CONVENTIONS

Transmitting digital information from one location to another and to provide a signal isolation from noise sources are key issues in a digital system design [3]. Another major aspect is to provide accurate transmitter and receiver references for the signaling system. Hence, noise in either one of the references corrupts directly the signal. Therefore, current-mode signaling is preferred over the voltage-mode signaling, since it is difficult to provide an accurate voltage references that are isolated from the power supply noise for the small signal swings used in efficient signaling systems [5].

2.1. Differential signaling

A binary signal can be transmitted differentially over a pair of conductors by driving one conductor with the signal and the other one with the complement of the signal. Therefore, the transmitter references are less critical, since the receiver compares two voltage levels rather than comparing a voltage to a fixed reference. Furthermore, the voltage swing between '1' and '0' is twice as much compared to single-ended signaling which gives larger noise margin and a speed advantage [3]. The transmitter / receiver pair used for current-mode differential signaling is shown in Figure 1.

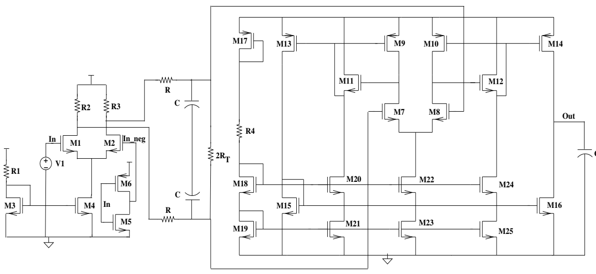

Fig. 1. Differential current-mode transmitter / receiver.

The transmitter has a source coupled current steering driver with a small resistive load, which is used to decrease the voltage swing of the line. A simple current mirror is used for biasing the source coupled pair. The receiver is a single-stage class-AB differential amplifier, which consists of NMOS source-coupled differential pair biased by a cascode current sink [8]. The transistor sizes and detailed description of the system can be found in [10].

The transmitter / receiver circuits for voltage-mode differential signaling are shown in Figure 2. The transmitter has a low voltage swing and its operation is energy efficient since it uses NMOS transistors for both pull-up and pull-down. However, the operation of the receiver amplifier is completely complementary. Each n-type device operates in push-pull fashion with a corresponding p-type device and it it self-biased through negative feedback [2].

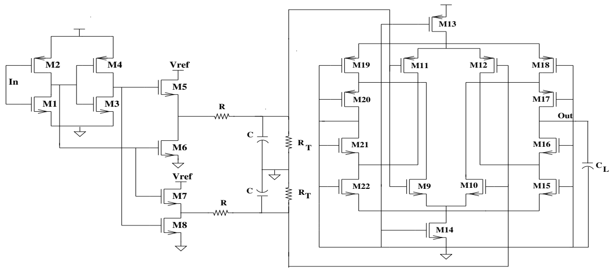

Fig. 2. Differential voltage-mode transmitter / receiver.

2.2. Simultaneous bidirectional signaling

The simultaneous information transfer in both directions over the transmission line has long been used in telephony. In ULSI design the effective wire density and pin count of the system can be doubled by sending bits simultaneously in both directions [6]. The simultaneous bidirectional transmitter / receiver were implemented using current-mode signaling due to its superior performance over the voltage-mode simultaneous bidirectional signaling [5, 8]. Terminations in both ends of the transmission line provides added immunity for both power supply noise and crosstalk.

The transmitter for simultaneous bidirectional signaling, shown in Figure 3, is designed to drive a current signal onto a transmission line and an identical current signal through a dummy load. The receiver, shown in Figure 4, is a single-stage class-AB differential amplifier. The amplifier consists of a NMOS source-coupled differential pair biased by a cascode current sink. The detailed description of these implementations can be found in [10].

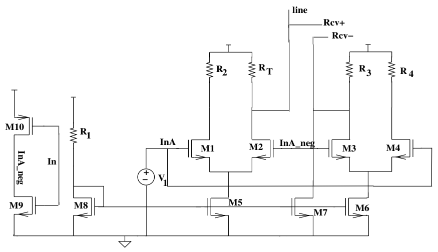

Fig. 3. Transmitter portion of the simultaneous bidirectional signaling transceiver.

3. CASE STUDY 1: VITERBI DECODER

The path metric unit (PMU) is the core of the computation in Viterbi decoder. Therefore it dominates the overall power consumption. For instance with a random input bit sequence the power

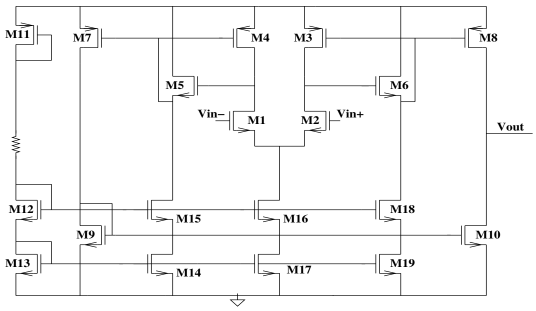

Fig. 4. Receiver portion of the simultaneous bidirectional signaling transceiver.

dissipation of the PMU can be as high as 90 % of the overall power consumption [12]. This motivates to concentrate design efforts on the PMU in order to smoothen the current profile of the circuit. By adopting asynchronous design methodology, the high current peaks caused by a clock induced switching can be decreased and therefore the power supply noise is reduced [9].

The synchronous PMU [13], shown in Figure 5, consists of eight processing elements. The interconnects between processing elements were implemented using three different methods, asynchronous, time-interleaved and four-phase dual-rail [11]. In the time-interleaved data-transmission the message is divided into four four-bit groups, for instance if 16-bit message is divided, the bits 0,4,8,12 are the first group. This gives several benefits compared to a fully synchronous interconnect, firstly it decreases the simultaneous switching activity, which reduces the power supply noise. Secondly, adjacent bits do not switch simultaneously which suppress the crosstalk noise.

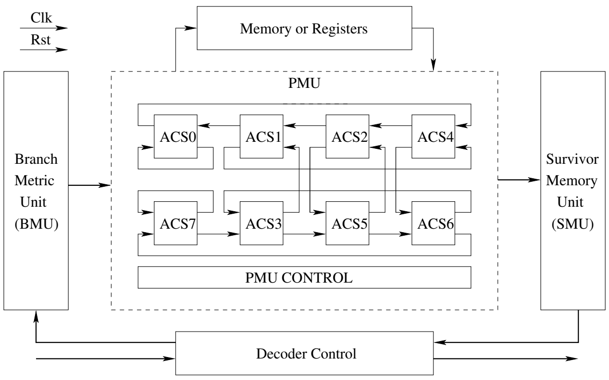

Fig. 5. The structure of the viterbi decoder.

In this paper, the presented current-mode signaling conventions are applied to the interconnects between processing elements. The length of the interconnect is 0.3 mm and the simulations are performed using 0.18 μm technology. The simulations results are compared with the conventional voltage-mode implementation, which is more commonly applied to local busses. The capacitance (C) and resistance (R) values used for the lumped RC model are result from the place and route performed with the Cadence Silicon Ensemble. The coupling capacitance (C_c = 16 fF) was calculated from technology data sheets.

The 16-bit interconnects from the path metric unit (PMU) were simulated using the worst-case switching activity. The peak current values are tabulated in Table 1 and the power consumption is shown in Table 2.

Table 1. Peak current values of the 16-bit interconnect (l=0.3 mm)

	I_{Peak} [mA]		
Design	Sync.	Interleaved	Dual-Rail
Volt.	7.4	2	9
Diff.	65	17	34
Bidir.	76	20	-

Table 2. Power consumption of the 16-bit interconnect (l=0.3 mm)

	Power [mW]		
Design	Sync.	Interleaved	Dual-Rail
Volt.	0.10	0.13	0.44
Diff.	160	160	380
Bidir.	243	243	-

The results shows that, the self-timed approach increases both the low-power and the low-noise behavior of the system. Furthermore, for the local interconnects, the conventional voltage-mode signaling has better performance in terms of power consumption and delay over the current-mode signaling conventions. Finally, the delay of the 16-bit interconnect is analyzed with different switching patterns, shown in Table 3. The two interconnect delays of one bidirectional line are marked as A and B. The line number seven is used as a victim line, while the rest of the lines acts as an aggressors. The results show that current-mode differential signaling has ability to suppress crosstalk and at the same time potential to provide equally fast data transmission than voltage-mode signaling.

Table 3. The influence of switching patterns to interconnect delay (l = 0.3mm).

		Delay [ps]		
Design	Pattern	Sync.	Int.	Dual-Rail
Volt.	↑↑↑	269	299	435 (1) 449 (0)
	↑↑↓	322	402	448 (1) 386 (0)
	↑↓↑	529	327	390 (1) 386 (0)
Diff.	↑↑↑	302	278	417 (1) 410 (0)
	↑↑↓	301	279	416 (1) 407 (0)
	↑↓↑	302	285	392 (1) 427 (0)
Bidir.	↑↑↑	452 (A)	389 (A)	-
	↑↑↑	378 (B)	418 (B)	-
	↑↑↓	456 (A)	391 (A)	-
	↑↑↓	380 (B)	411 (B)	-
	↑↓↑	455 (A)	389 (A)	-
	↑↓↑	383 (B)	410 (B)	-

Similarly, the eight interconnects of the PMU are simulated for power consumption and power supply noise, as illustrated in Tables 4 and 5. The average switching activity of the PMU is expected. When the eight interconnects are implemented using time-interleaved voltage-mode signaling, the reduction in peak current values is 92 % and the decrease in power consumption is 28 % from the synchronous voltage-mode implementation. In bidirectional signaling, the power dissipation of the interconnect is greater than others due to two sides termination, circuit complexity, and having two transceivers with replica drivers. However, the effective wire density and pin count of the system can be doubled using bidirectional signaling. In terms of power consumption and noise, the results show that for the local busses, the conventional voltage-mode signaling should be used along with self-timed communication.

Table 4. Peak current values of eight 16-bit interconnect (l=0.3 mm)

	I_{Peak} [mA]			
Design	Sync.	Async	Interleaved	Dual-Rail
Volt. Mode	18.7	2.9	1.4	3.8
Diff. Curr.	94.8	12	6.9	37
Bidir. Curr.	137	20	13	-

Table 5. Power consumption of eight 16-bit interconnects (l=0.3 mm)

	Power [W]			
Design	Sync.	Async	Interleaved	Dual-Rail
Volt. Mode	0.14m	0.14m	0.1m	0.4m
Diff. Curr.	1.3	1.3	1.3	3
Bidir. Curr.	1.9	1.9	1.9	-

4. CASE STUDY 2: GLOBAL ON-CHIP BUS SEGMENT

The presented signaling conventions were applied to a global on-chip bus segment, where the length of the bus varies from 0.25 mm to 3 mm. The resistance and capacitance values for the lumped RC-model were calculated according to the technology data sheets [10]. The simulations are performed using 0.18 μm technology and the worst-case switching activity is expected. Table 6 shows peak current values and power consumption for single driver / receiver pair for the both current-mode signaling conventions.

Table 6. Peak current and power consumption with variable interconnect lengths for one driver / receiver pair.

	D. Curr		Bidir.	
L [mm]	I_{Peak}[mA]	P[mW]	I_{Peak}[mA]	P[mW]
0.25	3	10	7.5	29.2
0.5	2.9	10	7.8	29.3
1	2.69	10.1	8.5	29.3
1.5	2.65	10.1	7.9	29.3
2	2.63	10.2	8.2	29.4
2.5	2.63	10.2	8.1	29.5
3	2.63	10.2	8.9	29.5

The results shows that, differential current-mode signaling has better performance in terms of power consumption and power supply noise over the bidirectional one. However, the differential current-mode signaling needs two lines for sending one signal while the bidirectional one uses one line for two signals. Therefore the effective wire density and pin count of the system can be doubled using bidirectional signaling. The variation in power dissipation and peak current values are quite small, when the line length varies from 0.25 mm to 3 mm. This indicates that their performance is not as dependent on the length of the line as it is with conventional signaling. Hence, conventional signaling needs number of traversals to drive the line and dissipates large amount of power.

The 16-bit bus segment was simulated and analyzed for power supply noise and power consumption, as shown in Table 7. The reference signaling technique, that is voltage-mode differential signaling, was not able to drive the line fully. This is shown as a decrease in power consumption when the length of the bus is increasing, which is not the expected behavior. The lumped RC-model, shown in Figure 2, has $R + R_T$ resistors in series. Thus, to drive this load, the pull-up transistors width should be increased over 100 μm which is not allowed in 0.18 μm technology. Therefore, in order to guarantee reliable data transmission, repeater insertion is necessary, which increases the power consumption and peak current of the system. Thus, in this case study, for voltage-mode differential signaling the repeaters should be inserted when the interconnect length is around 1 mm or higher.

Table 7. Performance of the 16-bit bus (l=2 mm).

	I_{Peak} [mA]	Power [mW]
Diff. Curr.	46	163
Bidir.	125	468

The current-mode signaling techniques have better performance in terms of power consumption and power supply noise over the voltage-mode signaling. The changes in power consumption for both bidirectional and differential current-mode signaling are small when the interconnect length increases from 0.3 mm to 2 mm. Hence in differential current-mode signaling the power consumption is the same regardless of the 1.7 mm increment in bus length.

The coupling between signals affects most to the voltage-mode differential signaling, as shown in Table 8. On the contrary, the differential current-mode is least affected by signal coupling. This result indicates that the current-mode differential signaling has ability to suppress crosstalk and to provide fast data rates. The two interconnect delays per one line, in bidirectional signaling, are marked as delay A and delay B.

Table 8. Influence of switching patterns to interconnect delay (l=2 mm).

	Pattern	Delay [ps]
Diff. Volt.	$\uparrow\uparrow\uparrow$	645
	$\uparrow\uparrow\downarrow$	621
	$\uparrow\downarrow\uparrow$	605
Diff. Curr.	$\uparrow\uparrow\uparrow$	467
	$\uparrow\uparrow\downarrow$	460
	$\uparrow\downarrow\uparrow$	446
Bidir	$\uparrow\uparrow\uparrow$	455 (A) 409 (B)
	$\uparrow\uparrow\downarrow$	540 (A) 472(B)
	$\uparrow\downarrow\uparrow$	613 (A) 548 (B)

The power supply noise and crosstalk can be decreased even more by applying self-timed design techniques as shown in the previous section. From the above discussion, differential current-mode and simultaneous bidirectional signaling has the best performance in terms of delay, power dissipation and noise for global on-chip wires.

5. CONCLUSION

Signaling conventions for global and local on-chip interconnects has been introduced in this paper, namely voltage-mode and current-mode differential signaling, and simultaneous bidirectional signaling. In the first case study these signaling techniques were applied to the 16-bit interconnects of the path metric unit in Viterbi decoder. In terms of power consumption and power supply noise, the conventional voltage-mode signaling is the most suitable for the local interconnects of the Viterbi decoder. The reduction in power consumption and noise is 28 % and 92 % respectively, when time-interleaving is applied to voltage-mode signaling. When considering delay, the differential signaling has a similar performance as the voltage-mode signaling. However, differential signaling has advantage to suppress crosstalk.

In the second case study, the presented signaling conventions were applied to a 16-bit global on-chip bus segment. The length of the interconnect varies from 0.25 mm to 3 mm. For the voltage-mode differential signaling, repeaters are required after the length increases over 1 mm, in order to guarantee reliable data transmission. In terms of noise, speed and power consumption, the performance of voltage-mode signaling is inferior compared with the current-mode signaling implementations. In both cases, by adopting the self-timed design methods, the study considered in this paper revealed the possibility to a significant noise reduction.

6. REFERENCES

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