Physical Performance Modeling for Platform-Based SoC Design

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Abstract-Ever increased demands for short time-to-market designs of microelectronic systems with increased complexity and integration density have implied that new design methodologies will be needed. In this article, we present a web-based course in electronics curriculum that answers to these demands and simultaneously supports the research co-operation between partner universities. Objectives for the course are presented and based on those a more detailed course content with a short description of each topic is given. Finally, a few words on the actual implementation of the course and its distribution through the web conclude the article.

1 Introduction

The current main electronic design trend is platform-based design integrating both the software and hardware components to a common architectural framework and supporting design methodologies. From the same architectural template, multiple instances, or products, can be generated, reflecting different feature set and natural evolution of the target implementation technologies. The driving forces behind this evolution have been increased product complexity in terms of hardware and software and enhanced user interfaces, strict time-to-market requirements for the whole process, enhanced intellectual property (IP) integration to specific design instances, and a need to maintain and develop the platform over multiple CMOS technology generations. These challenges combined with technology paradigm shift to deep sub-micron CMOS, imply that a more systematic and broader understanding of the system level physical issues is required. Such issues are e.g. power optimization, signal and power distribution integrity and communication throughput optimization. Additionally, technology scaling shifts the design paradigm from the design of functional blocks to the design of global communication schemes and an interconnect architecture. This results in a new kind of design concept, interconnect-centric design. The interconnect-centric design flow includes *a priori* signal integrity and power distribution estimates with cross-talk and power supply noise as constraints guiding the design of communication and power supply networks on the chip. Communication and synchronization will cost increasingly more over the operations themselves along the technology scaling. Thus, for system and architecture designers, the basic understanding over the inherent technology constraints and performance metrics will be of highest relevance, when selecting and designing the platform architectures and identifying their scalability and end product performance properties and constraints over the foreseeable

technology evolution and also the platform lifetime. The platform lifetimes, by definition, must exceed the platform instance, i.e. the product, lifetime.

In this paper, we propose objectives and a content for a jointly developed course addressing the system level view of the technological (electrical) aspects in the platform-based design. Within the course, recent research results from the participating research groups in three universities are encapsulated in the form of an advanced undergraduate/first year graduate course. The motivation for this kind of clustering in teaching comes from the joint projects, such as COMPLAIN [1] and SoC-Mobinet [2], between the universities that utilize teaching to support more strongly the research conducted in the laboratories. These kind of joint courses also close the knowledge gap and studying culture differences between the students in these universities.

In order to gain the best advantage of the course the student should have an earlier background on topics such as basic computer architectures [3], principles of digital design [4] and digital circuit design [5]. All these topics are dealt with in separate courses in electronics curriculum so these courses form a suitable ground for our course.

2 Course content

The main focus areas, or core components in our course, are 1) platform-based design concepts and methodologies, 2) technology scaling and the technology roadmap from system perspective, 3) performance estimation and modeling principles and techniques for evaluating different platform architectures.

Within the course we investigate how different electrical phenomena affect the system performance and how technology scaling and an interconnect-centric design methodology affect a partition of our heterogeneous system, allocation of its resources and mapping the resources on the hardware. The result is the suitable platform architecture for the need of an application.

The course **objectives** are that after the course a student should be able to a) understand *platform-based* design concept, b) analyze an impact of *technology scaling* (e.g. roadmaps) and different implementation technologies on the *system performance characteristics*, c) select a *suitable platform architecture* on a given technology for the specified task/application, d) understand different kinds of *modeling techniques and principles* and use them for the modeling of different case studies, e) understand the principles of *interconnect-centric design* and use them in modeling and designing the platforms.

In order to meet these objectives, the core components, jointly developed for this course are:

Course Content & Organization	(Prof. J.Isoaho)
ITRS Roadmap – critical performance metrics	(Prof. H.Tenhunen)
Modelling techniques and principles	(Prof. A.Jantsch)
Platform-based design and platform architectures	(Prof. J.Isoaho & J.Nurmi)
Interconnect-centric design	(Dr. L.-R. Zheng)
Early estimation of system level performance	(M.Sc. T.Nurmi)

The roadmap part follows closely the predicted industrial technology evolution in CMOS towards a year 2010. Instead of focusing the process or device parameters, we cover the relevant issues and impacts from the architectural and system point of view. The performance metrics includes the standard throughput metrics, signal integrity, reliability, and strategic yield/manufacturability issues relevant to CMOS technologies below 0.1 micron.

Modeling is an integral part of many design activities from the system level to the circuit level. The fundamental principles of modeling, such as *state* and *event*, are introduced and we investigate a number of ways to categorize a system by its characteristics (linear and non-linear, or static and dynamic, etc). Then we review a selection of main modeling concepts. *Finite state machines (FSM)* are the classic modeling tool for representation and analysis of behavior. After a basic introduction to the FSM theory we discuss the fundamentally tight relation of FSMs to grammars and languages which turns out to be of great practical importance. *Grammars and languages* are a natural notation for describing communication protocols. Due to the tight correspondence between FSMs and grammars designers can use a grammar to specify a protocol and use an FSM for an efficient implementation. *Petri nets* are the classic tool to model and analyze concurrency and abstract performance issues. After introducing the basic Petri net theory we use the static scheduling of a set of processes on a single and multi-processor architectures as a practically useful application [6].

The fundamentals of platform-based design are introduced from a designer's perspective. The function of a platform-based design concept is to link a functional specification of a system to a tentative physical architecture, which is described as virtual engines characterized with a set of parameters. In modeling the inter-block communication is analyzed in more detail, as function blocks are considered more or less black boxes. The platform instance is generated for a particular application after careful design space explorations (within the platform parameter set), which includes performance, cost (i.e., size), power consumption, and noise analyzes. The intersection of the constraints by an application itself and the semiconductor technology defines the potential platform instances for the given specification [7].

The rapidly changed technology parameters in deep sub-micron and nanometer technologies have imposed a design method shift towards the one in which interconnect related physical/electrical effects must be considered in each level of the design flow. In an interconnect-centric design, we first introduce the interconnect strategies in SoC, analyze interconnect related deep sub-micron effects such as interconnect delay, signal and power integrity and noise-on-delay effects. Then, we explore the interconnect constraints on SoC performance which is followed by an introduction to basic techniques in coping with interconnect effects. After this, we present interconnect centric SoC architectures, which include on-chip signaling issues, synchronization and clock distribution, power distribution and chip placement plan [8], [9]. Finally, the interconnect-centric design methodology, which covers from *a priori* signal and power estimations to post layout verification, is reviewed [8,10]. During the theoretical studies, design and analysis examples are given for different optimum design objectives for SoC platforms.

Finally, early estimation of system level performance is introduced with two well-known system level physical/electrical models [11,12]. Both models use modular modeling hierarchy from transistor/gate-level to system-level (chip/package/module). A set of analytical equations is derived in both models, and different parameters relating to architecture platform and technology are used as model input parameters. By using all the methods presented earlier during the course the student can explore a design space for a case study platform instance.

3 Implementation

The targeted format for the course will be web-based, including the lecture, exercise and laboratory work distribution over the Internet. The lectures are presented in front of

a video camera. During the taped presentation, a SMIL-script is generated detailing the timings of each slide. This is done completely within MS PowerPoint™, and as the timings are recorded, the slides can be shown to the audience via data projector. Later the students can follow the lecture by using a suitable viewer, e.g. RealPlayer™[13], and are able to follow the video of the lecture in one part of the screen and the related slides in another one. An ISDN connection, a sound card and any processor of type of PII or later are minimum requirements to follow the lecture properly.

The exercises are also given through the web and the final documents are then returned by an e-mail to the assistant. The web-based distribution of both lectures and exercises enables each participating group to do the additional local variations in the course format and content, as well as releasing partner university faculty from excessive traveling in delivering the specific content in their expertise area.

4 Conclusions

In this article we presented a course concept that relies on the core that is common for all partner universities. Each university can then modify the actual course implementation and emphasize on different issues depending on the research direction. The objects for the course were derived based on the fact that design of the future microelectronic systems meets tightened demands for short time-to-market with increased complexity and integration density due to a large variety of versatile applications. The impact of technology on system performance metrics is highlighted and some modeling techniques and principles are presented. Issues, such as platform-based design, interconnect-centric design and early estimation of physical and electrical performance of the system, are explained. Finally, all these concepts are combined and used for a design of different platform instances for a suitable target application project. We sum up the article by telling a few words on the actual implementation of the course and its distribution through the web.

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