Architectural modeling of pixel readout chips Velopix and Timepix3

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We examine two digital architectures for front end pixel readout chips, Velopix and Timepix3. These readout chips are developed for tracking detectors in future high energy physics experiments. They must incorporate local intelligence in pixels for time-over-threshold measure-ment and sparse readout. In addition, Velopix must be immune to single-event upsets in its digital logic. The most important requirements for both chips are pixel size, timing resolution, low power and high-speed sparse readout. We describe the transaction level architectural models of the chips using SystemVerilog. The correctness of the models is ensured using Open Verification Methodology. We will also discuss the advantages gained from transaction level modeling.