RF Transceiver Circuit Technology Based Wireless Interconnects for Inter- and Intra-Chip Communication System

Cheng Tao, Peltonen Teemu, Tjukanoff Esa, Hannu Tenhunen
Department of Information Technology, University of Turku, Joukahaisenkatu 3-5 B, 20520 Turku, Finland;
Email:chetao@utu.fi; tejupe@utu.fi; esa.tjukanoff@utu.fi; hannu@imit.kth.se; Tel: +358-2-3338646; Fax: +358-2-3338600

ABSTRACT

In this work, some most frequently studied interconnect solutions in recent years have been discussed and compared to show their advantages and limitations. RF wireless interconnect (RFWI) method is further studied by system modeling in simulink environment and successful communication between transmitter and receiver is obtained. The results indicate the potential feasibility and reliability of the inter-chip and intra-chip communication system using integrated RF transceiver and antenna to replace the present metal wiring interconnect. The fact that lots of the existing experiences on RF transceiver and antenna design makes RFWI an attractive interconnect solution.

I. INTRODUCTION

With the increasing integration density and operation frequency of CMOS integrated circuits in the era of sub-100nm, the traditional metal wiring interconnect technology is emerging as the major bottleneck to the performance improvement of VLSI system such as System-on-Chip (SoC), System-in-Package (SiP) and Network-on-Chip (NoC) etc. This limit is due to the global interconnection delay becoming significantly larger than the gate delay. Figure.1 shows the relationship between gate and interconnect delay under different technology [1]. It is clear from this figure that under 0.18μm technology, interconnect delay dominates the speed performance. To address this challenge, a variety of new interconnect concepts and radical solutions have been developed during the past ten years.

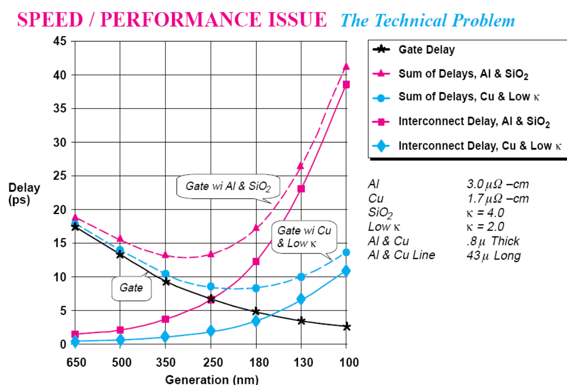


Fig.1 Delay .vs. Technology Node

In Section II, a short introduction is given on non-wiring interconnect solutions which have been proposed recently. The benefits and drawbacks of these interconnects are compared each other. The concept of RF/Microwave wireless interconnects through free space is discussed in Section III and a simple simulink model of RF transceiver is developed to demonstrate it. Section IV summarizes this work and gives a insight for future interconnect solutions.

II. NON-WIRING INTERCONNECT SOLUTIONS

Although the global RC delay is a major factor for metallic wiring, there are other factors that need to be studied especially when technology scales down. The signal integrity associated with the decreased geometries and power supply, increased clock and data frequency have become highly sensitive issues for low power applications of all kinds of circuits. These trends are a strong function of design strategy, and should be considered in that context.

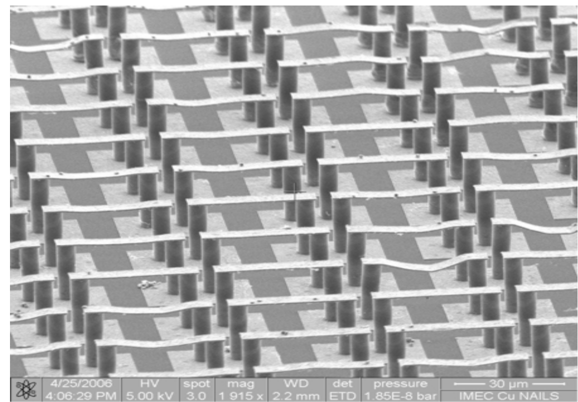


Fig.2 Through-Silicon-Via Chains for 3-D Stacked IC (Source: IMEC)

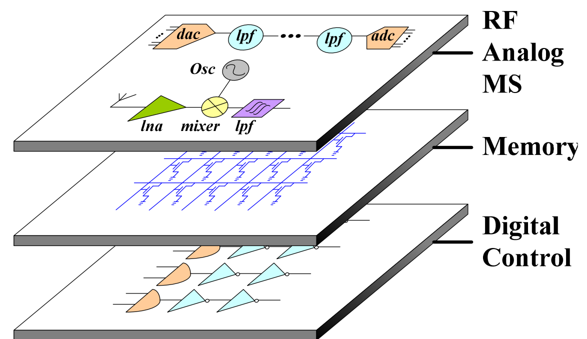


Fig.3 Hybrid Circuit Integration Concept

A. Through-Silicon Via Technique

3-D chip stacking using high density through-silicon vias (HDTSV) (see Fig.2) is a key focus area for improving delay and power in addition to providing increased functional diversity for chip assemblies.

In 3-D ICs the circuits are split up into smaller units and stacked, making it easier to avoid the long-wiring problem. This, not only reduces the interconnection length between devices by the short vertical wiring with very small via dimensions, but also makes it possible for heterogeneous technology (Si, GeSi, GaAs; bipolar and CMOS) and hybrid circuit (RF/analog/MS, digital) integration (see Fig.3). According to 2007 ITRS [2], as much as 50% reductions in global interconnect length and die area can be achieved. This

corresponds to a 4× increase in clock frequency and 2× reduction in interconnect power dissipation.

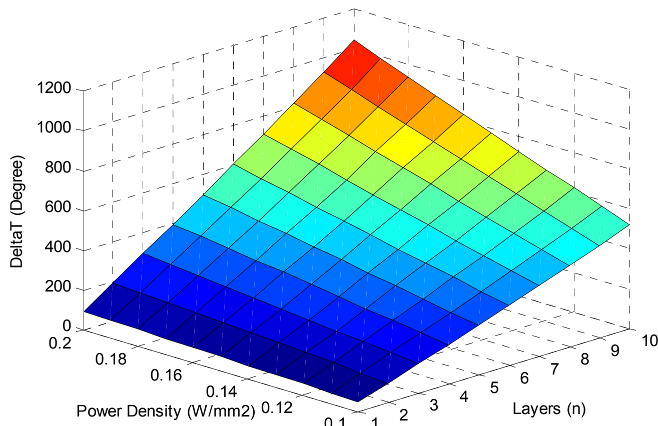


Fig.4 Temperature increase as a function of n and the power density in each layer

Even though, it is an attractive technique in process field, TSV has not gone commercial by far due to so many technical and cost issues. One of these issues is etching process to form small-diameter vias with smooth sidewalls, controllable sidewall angle, and minimal mask undercut. Alignment accuracy is also critical for wafer-to-wafer process to get high-density interconnect. In addition, Heat-sinking technology should be found for heat removal to solve the problem of sharp increase in power density of 3-D chips. It shows the temperature variation with the power density and chip layers in Fig.4.

B. Optical Interconnects

Optics offers light-speed transmission without the frequency dispersion and loss associated with electrical wiring. So it can supply high bandwidth, large data throughput and excellent signal integrity property with quite little EMI, signal reflection and noise problem [3-4]. For example, in [5], the measured BW is 1.01GHz, making each channel suitable for operation up to 1.5Gb/s and the total data throughput reaches 96Gb/s for 64 channels. Also electrical and substrate crosstalk rejection is better than 40dB across the BW.

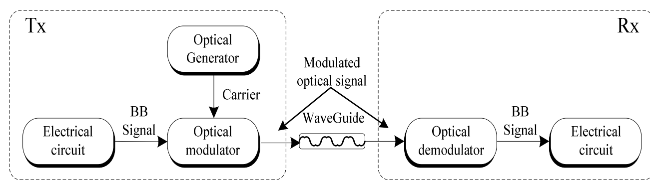


Fig.5 A Simple Case for Optical Interconnects

Nevertheless, it is inevitable to transform signals between electrical and optical form as can be seen from Fig.5. This is due to the requirements for light generator at Tx part such as vertical-cavity surface-emitting laser (VCSEL) and photo-detector (PD) at Rx part [5] as well as an on-chip waveguide. In some cases, couplers or splitters are used to bring light from external sources into package and die or divide a light source into two or more waveguides. Furthermore, new circuit blocks and design methodology are needed such as optical modulator and demodulator. Special packaging process and technology are also necessary. For example, in [5], the BiCMOS process for laser driver array and TIALA array, and GaAs process for PD array are indispensable. All of these requirements lead to the fabrication difficulty and high cost. At least in the near future, on-chip optical interconnect techniques still need more research efforts.

C. AC Coupling

Interconnect system based on capacitive and inductive coupling, known as AC coupling, has been largely studied in recent years as an alternative for metal wiring interconnect. This type of system is shown in Fig.6.

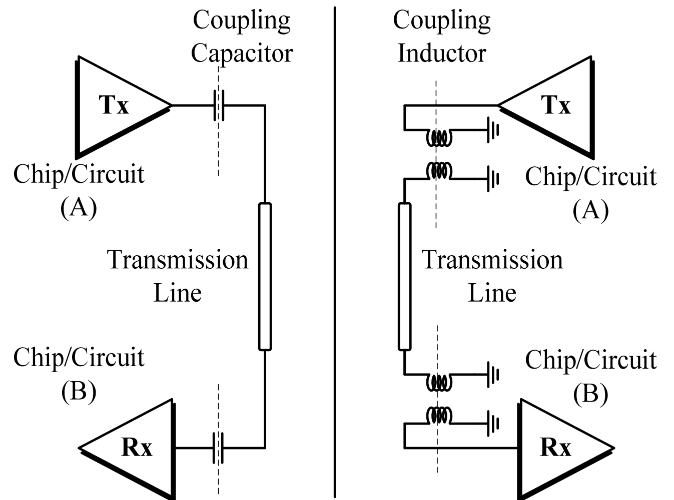


Fig.6 AC Coupling System Model

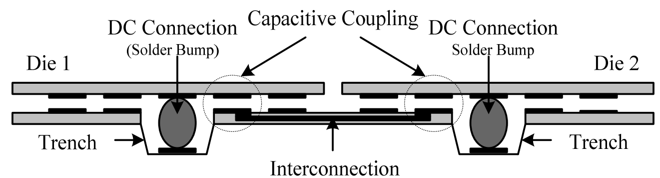
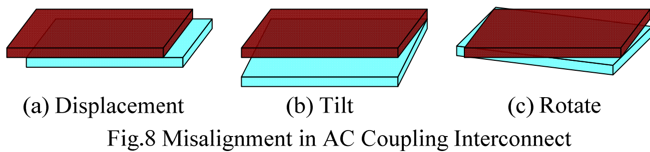


Fig.7 Capacitive Coupling Based on Buried Bump

Table.1 AC Coupling Performance Comparison

	[9]	[10]
AC coupling	Inductive	Capacitive
Date Rate	11 Gb/s	11 Gb/s
Distance	15 μm	3 μm
Energy	1.4 pJ/b	0.39 pJ/b
Channel Area	0.015 mm^2	0.016 mm^2
BER	$<10^{-14}$	1.02×10^{-14}
Modulation	Pulse	25 GHz ASK
Process	0.18 μm	0.13 μm

Compared to TSV and optical techniques, no extra manufacturing and packaging process and special circuits are needed for AC coupling mechanism. It enables multi-gigabit-per-second communication data rates with relatively high pin density and low power consumption. One possible implementation of capacitive coupling is shown in Fig.7 [6]. Inductive coupling is superior to capacitive coupling in coupling strength through body, interference immunity, package flexibility and electrical scalability etc.[7]. Table.1 shows the performance comparison of two recent chips.



(a) Displacement (b) Tilt (c) Rotate

Fig.8 Misalignment in AC Coupling Interconnect

The inability of supporting long-distance (>1mm) transmission and the requirement of accurate alignment for BER performance become two prominent constraints on AC coupling system, because transmitting and receiving channels may become misaligned due to vibrations or thermal expansion of chips, as shown in Fig.8. To relax this limit, an electronic alignment correction technique [8] can be used but extra power consumption has to be dissipated. What's more, for capacitive coupling, transmission can only be realized between two chips, which greatly restricts its application.

III. RF WIRELESS INTERCONNECT (RFWI)

As explained above, AC coupling has provided so many potential properties in terms of data rate, realization simplicity and cost-efficiency. However, it is a kind of proximity data communication in nature, that is, devices or circuits are interconnected locally. In order to obtain even longer distance, RF transceiver with on-chip antenna technique can be used. That is RF transceiver based wireless interconnects (RFWI). Like AC coupling, there is no requirement for RFWI to make any process related modification. Since RF transceiver circuits have been tremendously researched in a variety of applications, a lot of design experiences can be taken from existing works. In this work, a transceiver demonstration system of 10-bit 2Gb/s data rate, 40GHz carrier frequency with on-off keying (OOK) modulation is developed.

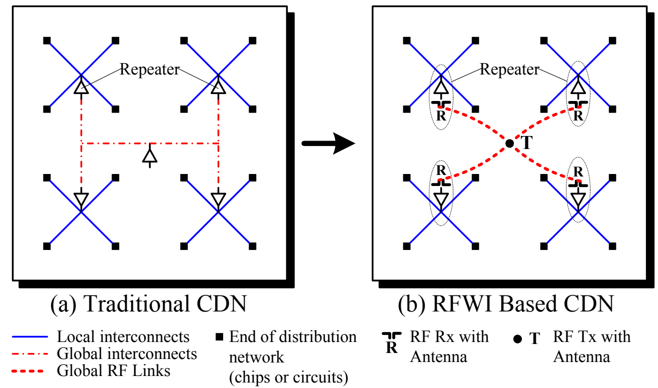


Fig.9 Traditional CDN .vs. RFWI Based CDN

A. System Concepts

The proposed RF wireless interconnect concept is explained in Fig.9. In traditional clock distribution network (CDN), global H-type wiring and repeaters are inserted between signal source and nodes. While in RFWI system, global wiring is replaced by the free-space channel with transmitter and receiver antennas at each side. Obviously, there is little requirement for alignment and restrictions on the number of devices or chips.

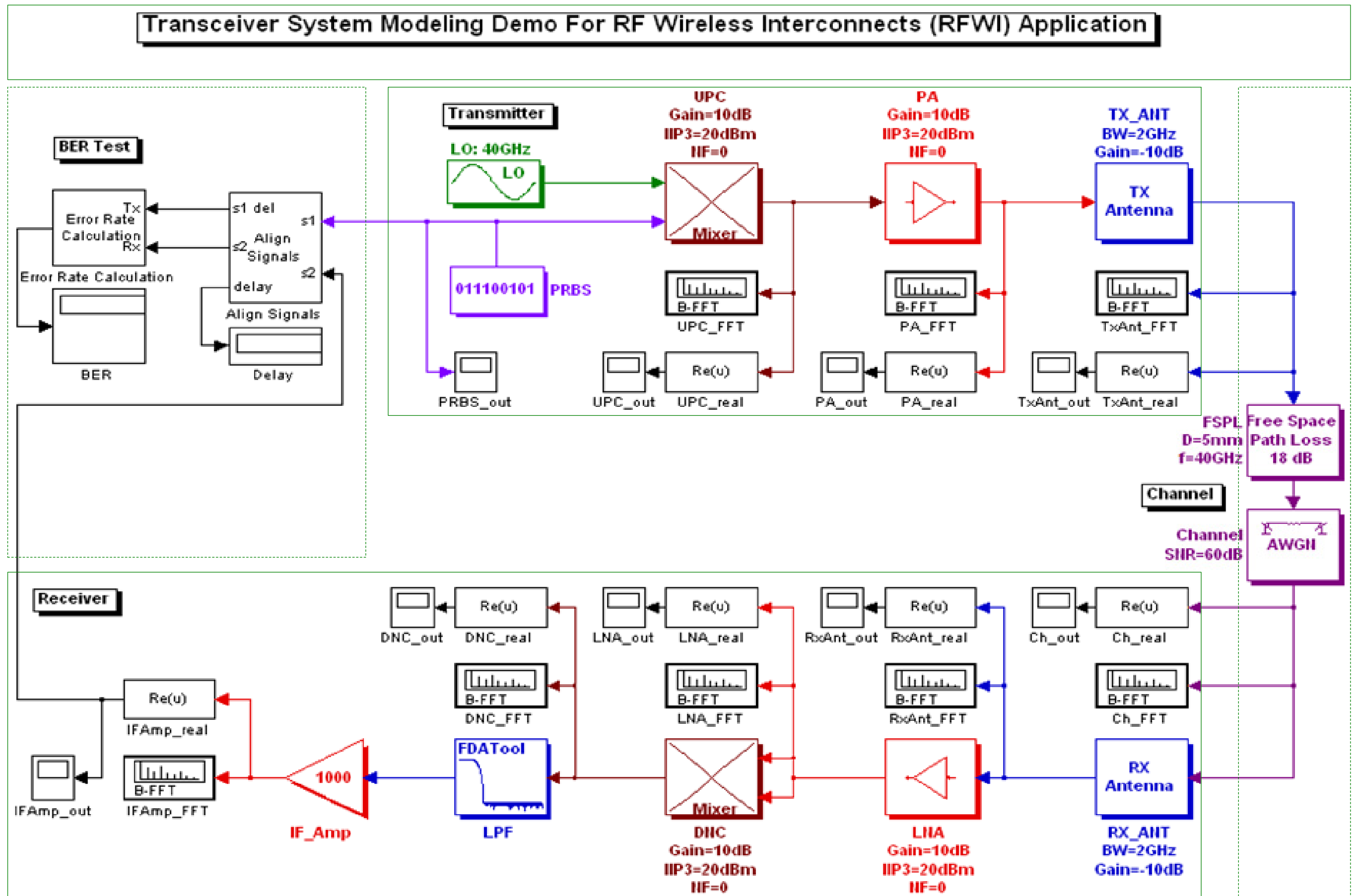
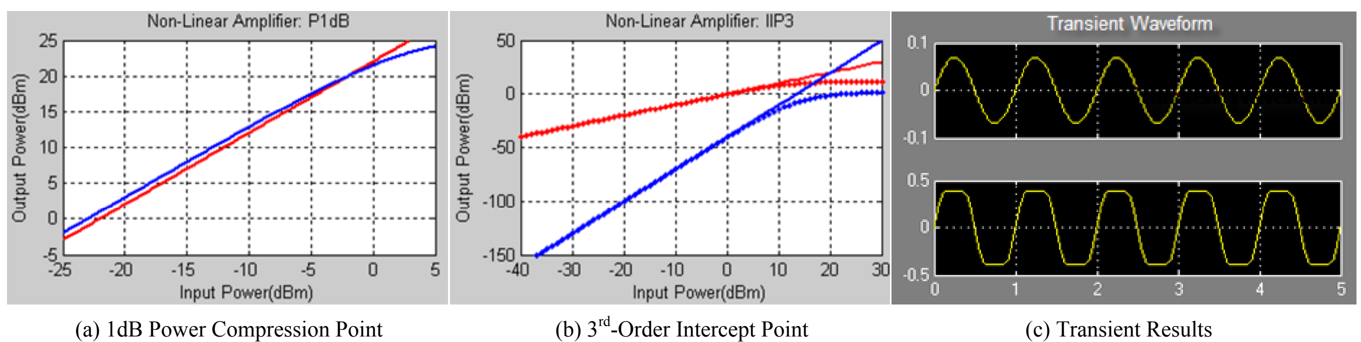


Fig.10 Transceiver System Modeling For RFWI Application

B. Simulink Modeling

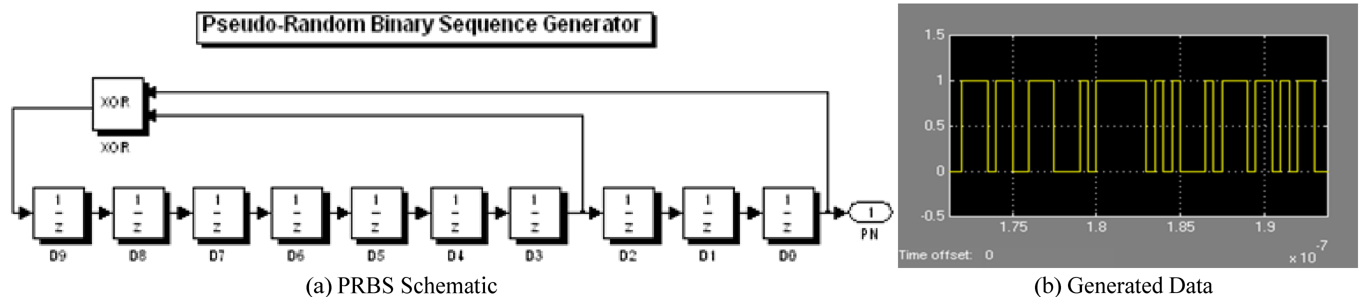
Based on the system concept explained above, a simple behavior model for RFWI has been designed as shown in Fig.10. The model consists of transmitter, receiver and channel. In this demo, the antennas at Tx and Rx part are replaced by two BandPass Filters (BPF) with -10dB voltage gain. While the signal propagation channel is modeled by free-space path loss (FSPL) followed by an AWGN block, which can fulfill the basic operation without affecting the accuracy of the analysis. The FSPL parameters are decided by the equation: $L(dB)=32.5+20\times\log(D)+20\times\log(Fc)$. For 5mm device or chip distance ($D=5\times10^{-6}$ km), the path loss under 40GHz center frequency ($Fc=4\times10^{4}$ MHz) is about 18dB.

The power amplifier (PA) and low noise amplifier (LNA) are both modeled by mathematical RF amplifier module in RF Blockset. Figure.11 has shown the result of 1dB power compression point (P1dB), 3rd-order intercept point (IP3) and



(a) 1dB Power Compression Point (b) 3rd-Order Intercept Point (c) Transient Results

Fig.11 Nonlinear Performance Simulation for RF Amplifier



(a) PRBS Schematic (b) Generated Data

Fig.13 10-Bit PRBS Generator

transient simulation respectively. The mixer, shown in Fig.12, is implemented by an ideal multiplier, considering non-ideal behavior such as LO leakage, gain compression and intermodulation. Leakage path is controlled by a “Leakage Gain” and “Leakage On-Off” stage. The “Mixer Nonlinearity” block is used to model P1dB, IP3, noise figure (NF) and other nonlinearities.

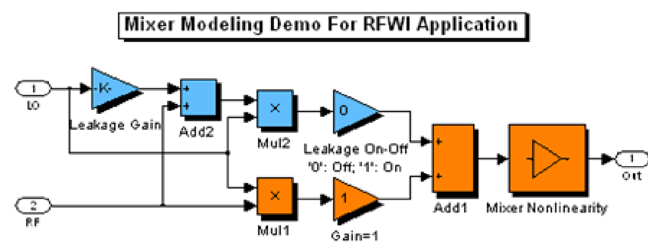


Fig.12 Mixer Model in Simulink

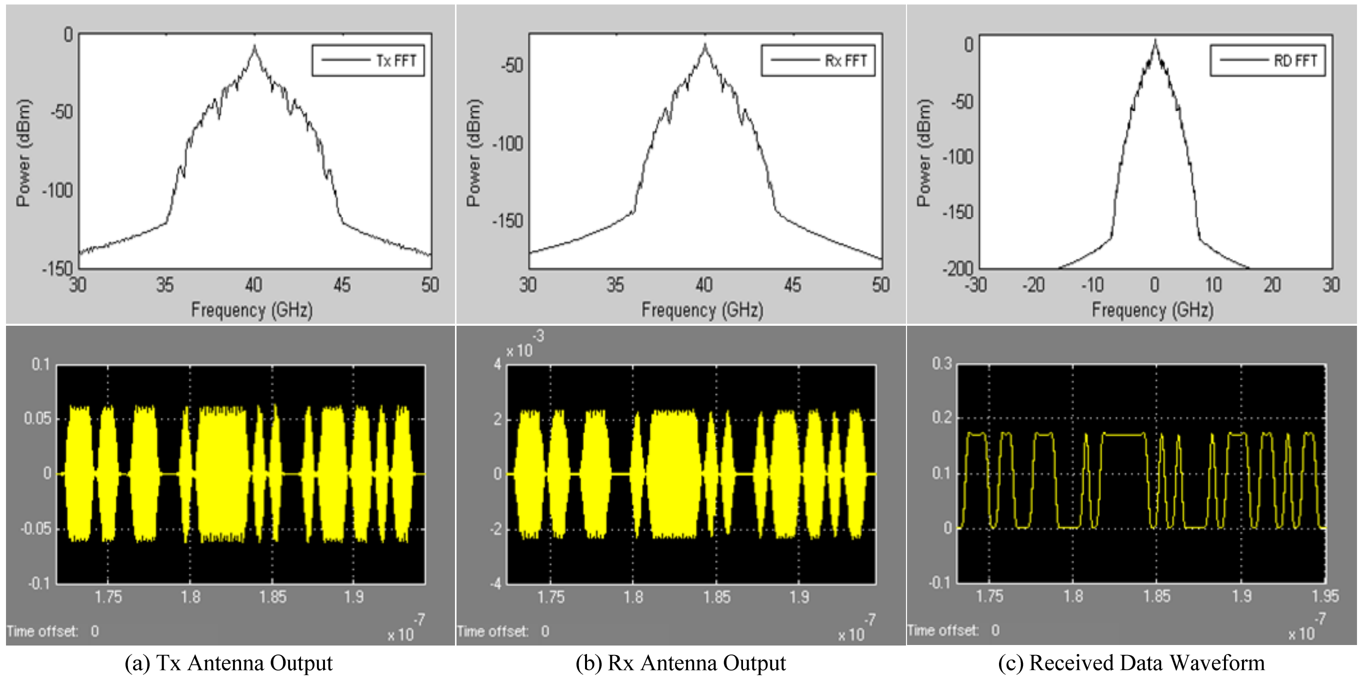
The baseband data used in this demo is a 10-Bit 2Gb/s pseudo-random binary sequence (PRBS). According to encoding theory, it can be created by using linear-feedback shift register (LFSR) as shown in Fig.13(a). The generator’s polynomial is: $x^{10}+x^{4}+1$. The baseband data generated by this module is shown in Fig.13(b).

C. Simulation Results and Conclusion

Given the ideal parameter configurations, the transmitted and received data waveforms in time and frequency domain are shown in Fig.14. from which we can see that the single tone 40GHz input carrier signal, modulated by 0-1 PN sequence (Fig.13b), is transmitted at Tx part (Fig.14a). At Rx part, the data is correctly received (Fig.14b) and demodulated (Fig.14c).

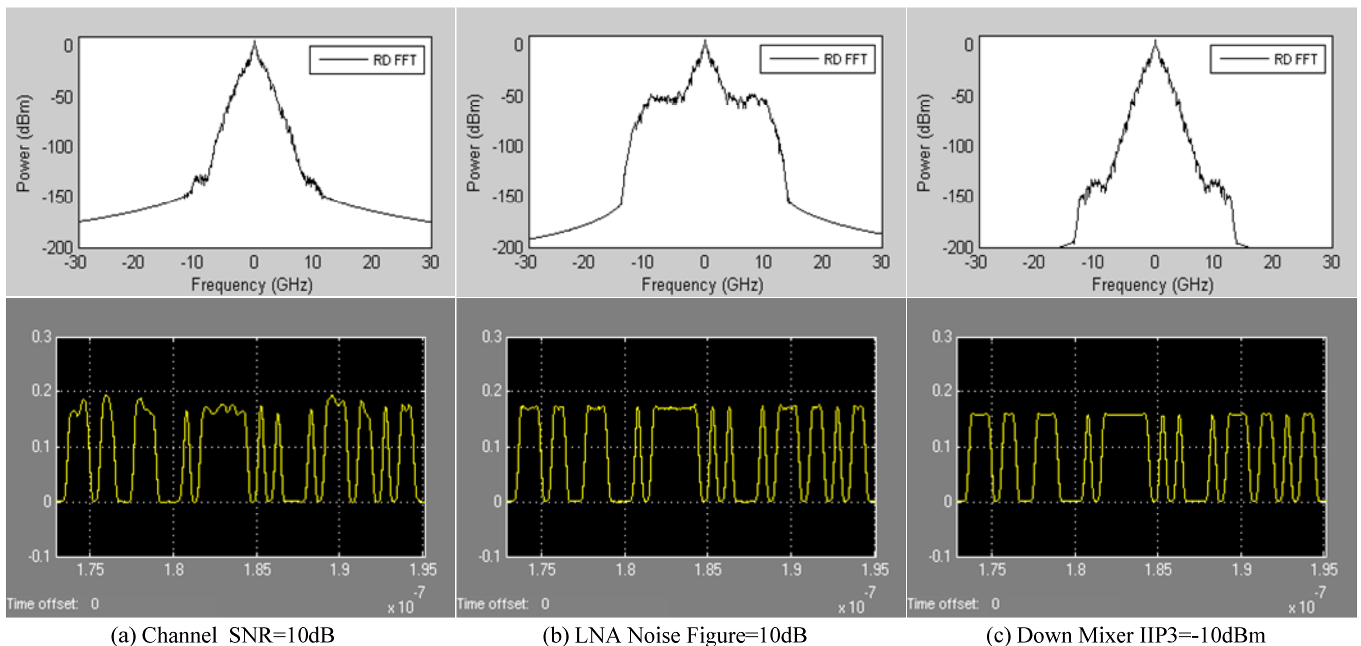
When considering the channel noise and nonideality of the circuit block, the performance of the system starts to go down. This is illustrated in Fig.15. We can see that system performance is very sensitive to the channel noise.

There are some practical issues and constraints that must be considered and resolved in the future research. One of the constraints is the challenge of designing an antenna with good performance and uniform characteristics. Let us look at Fig.9(b), it is important to guarantee that the four Rx antennas have nearly uniform performance, otherwise the received data might appear different in the four Rx circuits. In this case, Tx and Rx antenna must be isotropic ones. This is especially critical in designing the clock and data recovery (CDR) circuit. The other one is modeling of free space signal channel. More complex and complete models for free-space signal channel should be studied to include more non-ideal properties such as transmission path diversity.



(a) Tx Antenna Output (b) Rx Antenna Output (c) Received Data Waveform

Fig.14. Waveforms in Frequency and Time Domain for RF Transceiver System



(a) Channel_SNR=10dB (b) LNA Noise Figure=10dB (c) Down Mixer IIP3=-10dBm

Fig.15. Effects of Nonideal Circuit Parameters on System Performance

IV. SUMMARY

In this work, RF wireless interconnect has been proposed which has potential advantage over the most frequently researched non-wiring interconnects. In order to show the benefits of the proposed RF wireless interconnect, the advantages and limitations of through-silicon-via, optical and AC coupling interconnect schemes have been discussed and compared. Simulation of the RFWI interconnect is carried out and successful transmitting and receiving is realized using simulink modeling environment.

This work is still going on. Some more challenging researches are to be done in future. One of them is to model multipath effect and space noise in the signal channel. This non-ideal issue can severely degrade the quality of communication between chips or devices. The other one is to add more non-linear characteristics into each building block so that the actual operating state can be obtained. Besides, different modulation schemes are also required to be analyzed and compared to gain good BER performance.

This design approach finally requires a system-level integration viewpoint, combining the design, process technology, packaging, and board construction in the solution to achieve the desired performance and reliability.

REFERENCES

[1] The National Technology Roadmap for Semiconductors (NTRS), Semiconductor Industry Association (SIA), 1997.

[2] The International Technology Roadmap for Semiconductors (ITRS), Semiconductor Industry Association (SIA), 2007.

[3] M. Bamal, et al, "Performance Comparison of Interconnect Technology and Architecture Options for Deep Submicron Technology Nodes", IEEE International Interconnect Technology Conference, pp.202-204, Jun.2006.

[4] G. Q. Chen, et al., "On-chip Copper-based .vs. optical Interconnects: Delay Uncertainty, Latency, Power, and Bandwidth Density Comparative Predictions", IEEE International Interconnect Technology Conference, pp.39-41, Jun.2006.

[5] S. Goswami, "A 96GB/s-Throughput Transceiver for Short Distance Parallel Optical Links", ISSCC Dig. Tech. Papers, pp.230-231, Feb. 2008.

[6] S. Mick, et al, "4 Gbps High-density AC Coupled Interconnection," in Proc. IEEE Custom Integrated Circuits Conf. (CICC), pp.133–140, May 2002

[7] http://bwrc.eecs.berkeley.edu/Classes/ee290c_s07/

[8] R. Drost, et al., "Electronic Alignment for Proximity Communication", ISSCC Dig. Tech. Papers, pp.144-145, Feb. 2004.

[9] N. Miura, et al, "An 11Gbps Inductive-Coupling Link with Burst Transmission", ISSCC Dig. Tech. Papers, pp.298-299, Feb. 2008.

[10] Q. Gu, et al., "Two 10Gb/s/pin Low-Power Interconnect Methods for 3D ICs", ISSCC Dig. Tech. Papers, pp.448-449, Feb. 2007.