Impact of Circuit Non-Idealities on Wireless Interconnect Based on OOK Modulated RF Transceiver

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Abstract—In this work, a system model for RF wireless interconnect has been proposed based on digital on-off keying (OOK) modulated RF transceiver with 2Gb/s transmission rate and 40GHz carrier frequency. To evaluate performance of wireless interconnect, the impact of critical non-idealities caused by circuit blocks has been analyzed and simulated in Matlab[®] Simulink[®] environment. A set of rough circuit specifications and BER performances of such system are obtained, through which key points during actual circuit design has come into view. The result of this work has verified the potential feasibility and reliability, and pointed out possible circuit design stresses for wireless interconnect system.

Index Terms—System modeling, wireless interconnect, RF transceiver, on-off keying, BER, Matlab[®], Simulink[®]

1. INTRODUCTION

The essential development demand for wireless interconnect is the highspeed transmission regardless of the successive feature size scalingdown. In sub-100nm era, however, device density and clock frequency of circuits have rocketed up remarkably. The conventional metal wiring interconnect technology brings severe problems like increased delay, signal integrity and dynamic power dissipation, which is emerging as a major bottleneck to the performance improvement of VLSI system.

RF wireless interconnect, advanced about ten years ago, has recently been researched to a great extent to address the above problems in [1]-[7]. Nonetheless, few of these works build a model and make analysis at system level for data communication through wireless interconnect. As a

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part of overall design flow, a complete system should be modeled and simulated in the first place to find out what RF wireless interconnect is supposed to do and what factors will affect its normal operation. In virtue of modeling results, system performance can be transformed into detailed circuit-level specifications that will provide a brief insight into circuit design.

In this work, an OOK modulated RF transceiver system for wireless interconnect is proposed and evaluated under Matlab[®] Simulink[®], with emphasis on impact of block non-idealities to system BER performance. The paper is arranged as follows. Section 2 describes the architecture of RF transceiver model. In Section 3, modeling details for each sub-block have been supplied. A group of simulation cases and results are shown in Section 4. The last part, Section 5, has summarized this work.

2. RF TRANSCEIVER ARCHITECTURE

The proposed RF transceiver system model has been shown in Figure 1. The model is composed of transmitter (Tx), receiver (Rx), transmission channel (Ch) and some essential testing components. Balanced signaling scheme is used in this model.

The high frequency carrier signal (LO) and pseudo-random binary sequence (PRBS) signal ("td") are first converted into balanced form before they are modulated by up-conversion mixer (UpMixer). Then, the modulated signal is amplified by power amplifier (PA) and transmitted via transmitting antenna (Tx_Ant) to the noisy and lossy channel. In Rx path, the weak signal captured by receiving antenna (Rx Ant) is firstly



Fig.1 RF Transceiver System Modeling for RF Wireless Interconnect



Fig.3 Modeling of Mixer, Low Noise Amplifier, Power Amplifier and Local Oscillator

amplified and shift back to baseband respectively by low-noise amplifier (LNA) down-conversion mixer (DnMixer). Then the mixer's output is low-pass filtered (LPF) and buffered into the final single-end analog baseband (RxBB) data ("ra").

In order to compare the original Tx data with Rx data ("td" and "rd") for bit-rate error evaluation, the analog waveform is supposed to be sampled and quantized into digital data before sent to "Ber Test" block. Besides the above circuit blocks, some testing modules, like time and spectrum scopes and BER measurement block are embedded into the system.

3. MODELING OF CIRCUIT BLOCKS

To begin with, PRBS data generator is modeled. According to encoding theory, a 10-bit linear feedback shift register (LFSR) with polynomial $x^{10}+x^4+1$ can be used to generate Tx data. In order to emulate the finite rising and falling transition edge, an LPF is added after LFSR with the 1st-order transfer function $1/(1+s\cdot\tau)$ where $\tau=2.2$ Trf is the time constant and Trf denotes the rise/fall time [8]. Figure 2 shows the realization of PRBS and simulated data waveforms w/o transition edge control.

Mixer, illustrated in Figure 3(a), is simply realized by an ideal multiplier, considering non-ideal characteristics such as noise figure (NF), 1-dB power compression point (P1dB) and 3rd-order intercept point (IP3) which are modeled by cascaded RF amplifier (RFA).

PA, LNA and the nonlinear part of mixer are all built by mathematical RF amplifier module in RF Blockset® of Simulink®. A simplified RF amplifier is demonstrated in Figure 3(b) which consists of a gain stage, cubic nonlinearity and additive white noise. The results of P1dB, IP3 and transient simulation waveform have been provided in Figure 4.

Carrier is a real signal in practice. However, due to the complex input requirement of RF amplifier, it has been represented as the combination

of two conjugated complex signals with half of the LO actual amplitude: $0.5A \cdot (e^{+jx}+e^{-jx})$. As a critical parameter, phase noise must be added using Simulink® build-in module. Figure 3(c) shows the components of local oscillator. A plot of three different phase noises and their corresponding spectrums is also illustrated by Figure 5.

Wireless signal propagation in space is modeled as a free space path loss (FSPL) in series with an additive white gauss noise (AWGN) channel. The loss is decided by carrier frequency and antenna distance between Tx and Rx and calculated by $L(dB)=32.5+20 \cdot log(D)+20 \cdot log(Fc)$. So a 5mm distance (D=5×10⁻⁶ km) and 40GHz carrier frequency (Fc=4×10⁴ MHz) will lead to an 18dB loss. Additionally, to include the influence of adjacent-channel interference, a close-to-carrier single-tone sine signal is thereby injected to the channel to model such external non-ideal factors. Antenna is modeled by a band-pass filter (BPF) centered at carrier frequency with a loss stage. Although simple, this channel model is sufficient to reach our goal in this work.

Since the signal is transmitted and received in balanced form, so it is necessary to add single-to-balance (S2B) and balance-to-single (B2S) converters. B2S is just a subtracter while S2B can be realized by two out-phase gain stages with the gain value 0.5, followed by a delay cell on each branch. The delay can be adjusted to check its effect on system performance.

4. SIMULATION SETUP AND RESULTS

To verify the proposed system's function, ideal parameters are written to each module in the first place. The transmitted and received data in time domain and eye diagrams are shown in Figure 6(a). Another group of waveforms with large LO phase noise are also given in Figure 6(b) to make a comparison with the former one. Missing codes and error codes as well as unopened eye diagram are seen in this figure. Power spectrum





density (PSD) in Figure 7, plotted by superimposing one hundred frames data together with 1024 samples in each frame, are got at the output of Tx antenna, Rx antenna and buffer respectively. We can see from these figures that the PRBS data generated by Tx baseband (TxD) circuits can be correctly received and restored at receiver end.

When considering the channel noise and non-idealities of the circuit blocks, performance of wireless interconnect system starts to go down. In this work, six cases, shown in Table 1, are studied and simulated to explore system's failure mechanism. The six parameters to be explored are channel SNR, finite transition edges of PRBS data, adjacent-channel interference near the center of carrier, LNA IIP3, down mixer IIP3 and LO phase noise at 100KHz offset. In each simulation, the corresponding parameters take the range given in the column of "Range", while the other parameters are ideally set by column "Ideal values".

Due to the reason that the carrier signal is generated in sample mode, so the sampling frequency of simulation has been set to 409.6GHz. BER results for the above six cases have been provided in Figure 8, from which a clear view about system limiting factors has been indicated.

Table.1 Simulation Cases

Case Number	1st	2nd	3rd	4th	5th	6th
Non-Idealities	Channel SNR	Data Rise/Fall Time	Interference Power	LNA IIP3	DnMixer IIP3	LO Phase Noise
Range	0~18(dB)	$1.0 \sim 0.5(ns)$	-14 ~ -34(dBm)	$-19 \sim -9(\text{dBm})$	$-30 \sim -18(\text{dBm})$	$-60 \sim -80(dBc/hz)$
Ideal values	40 (dB)	Infinite	-100 (dBm)	20 (dBm)	20 (dBm)	-200 (dBc/Hz)



Table.2 Block-Level Specifications (based on BER<10⁻⁴)

Table 2 has summarized the rough block-level specifications for the RF transceiver model of this work which can be used as the foundation of practical circuit design. There are some practical issues and constraints that must be considered and resolved in the future research. One of the constraints is the challenge of designing an antenna with good uniform characteristics. If lacking of unification, the received data might appear discrepancy in different Rx circuits. In this case, Tx and Rx antennas are supposed to have isotropic traits. This is especially critical in designing clock and data recovery (CDR) circuit. The other one is the modeling of free space signal channel. More complex and complete channel models should be studied to include more non-ideal properties such as transmission path diversity. The multipath effects can cause jitters in received clock and Inter-Symbol Interference (ISI), which will severely degrade BER performance.

5. SUMMARY

In this paper, an OOK modulated RF transceiver system for wireless interconnect is modeled and simulated using Matlab[®] and Simulink[®], focusing on the evaluation of relationship between block non-idealities and system performance. Block functions and their non-ideal traits have been provided in detail to make the operation as practical as possible. Six different sub-block parameters—channel SNR, finite data transition edges, adjacent-channel interference, IIP3 of LNA and down mixer and LO phase noise, are considered and simulated to get BER performance and circuit limitations.

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